

# Implementing PID loop using FPGAbased platform: Case Study

**Kostiantyn Leontiiev, Technical Director**

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# Agenda

- RadICS Platform Overview
- PID Controller Implementation
- Implementation results
- Conclusions

# RadICS Platform Overview



# RadICS Platform Overview. HW

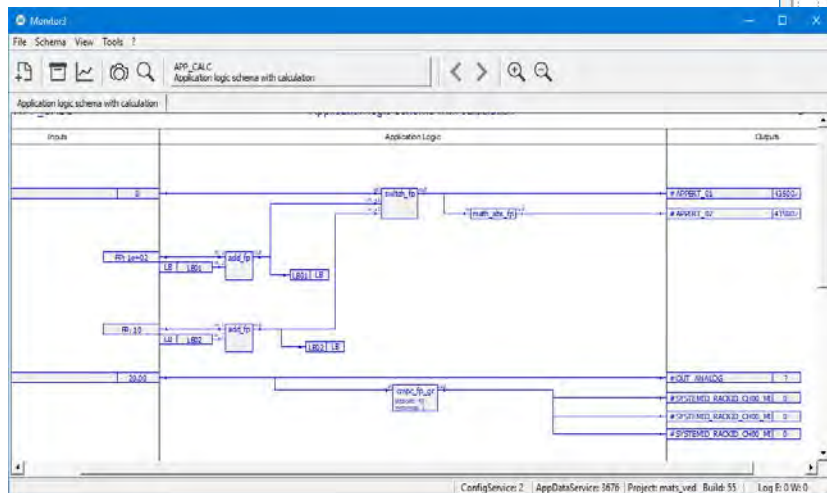
## Status update:

- FPGA-based
- Approved by US NRC to be used in safety I&C systems in USA
- IEC 61508:2010 SIL 3 architecture (in one chassis) was updated (including support SW)
- Three new modules were added (WAIM, TIM, RIM)



# RadICS Platform Overview. SW

→ RPCT Integrated Development Environment (IDE)



The screenshot shows the u7 - rpct\_user\_manual - Administrator application window. The title bar reads "u7 - rpct\_user\_manual - Administrator". The menu bar includes "File", "Administration", "Project", "Tools", and "?". The toolbar contains icons for file operations and a search icon. The main area displays a list of objects and their properties. The table below shows the data from the screenshot.

Object	EquipmentIDTemplate	Place	State
SYSTEM_1	SYSTEMID_1		Modify
RACK_1	\$(PARENT)_RACKID		Modify
Workstation	\$(PARENT)_WS00	0	Modify
Application Data Service	\$(PARENT)_ADS		Modify
Archive Service	\$(PARENT)_ARCHS		Modify
Configuration Service	\$(PARENT)_CFGs		Modify
Monitor	\$(PARENT)_MONITOR		Modify
TuningClient	\$(PARENT)_TUN		Modify
TuningService	\$(PARENT)_TUNS		Modify
CHASSIS_1	\$(PARENT)_CH\$(PLACE)	1	Modify
LM1-SF00	\$(PARENT)_MD00	0	Modify
Ethernet Adapter 1	\$(PARENT)_ETHERNET01	1	Modify
Ethernet Adapter 2	\$(PARENT)_ETHERNET02	2	Modify
Ethernet Adapter 3	\$(PARENT)_ETHERNET03	3	Modify
Opto Port 1	\$(PARENT)_OPTOPORT01	4	Modify
Opto Port 2	\$(PARENT)_OPTOPORT02	5	Modify
Opto Port 3	\$(PARENT)_OPTOPORT03	6	Modify
Input Controller	\$(PARENT)_CTRLIN	7	Modify
Output Controller	\$(PARENT)_CTRLOUT	8	Modify
Platform Interface Controller	\$(PARENT)_PI	9	Modify
DIM	\$(PARENT)_MDS\$(PLACE)	1	Modify
ADM	\$(PARENT)_MDS\$(PLACE)	2	Modify
ADM	\$(PARENT)_MDS\$(PLACE)	4	Modify
ADM	\$(PARENT)_MDS\$(PLACE)	7	Modify

The right pane shows the properties of the selected object, "Ethernet Adapter 1". The table below shows the data from the screenshot.

Property	Value
Common	
Caption	Ethernet Adapter 1
EquipmentID	SYSTEMID_1_RACKID_CH01_MD00_ETHERNET01
EquipmentIDTemplate	\$(PARENT)_ETHERNET01
Place	1
Network	
OverrideTuningDataWordCount	-1
TuningEnable	<input checked="" type="checkbox"/> True
TuningIP	192.168.31.1
TuningPort	50000
TuningServiceID	SYSTEMID_1_RACKID_WS00_TUNS

The status bar at the bottom right shows "Opened: 127.0.0.1".

→ Monitoring and Tuning System (MATS)

→ RPCT Outputs Verification Tool (ROVT)



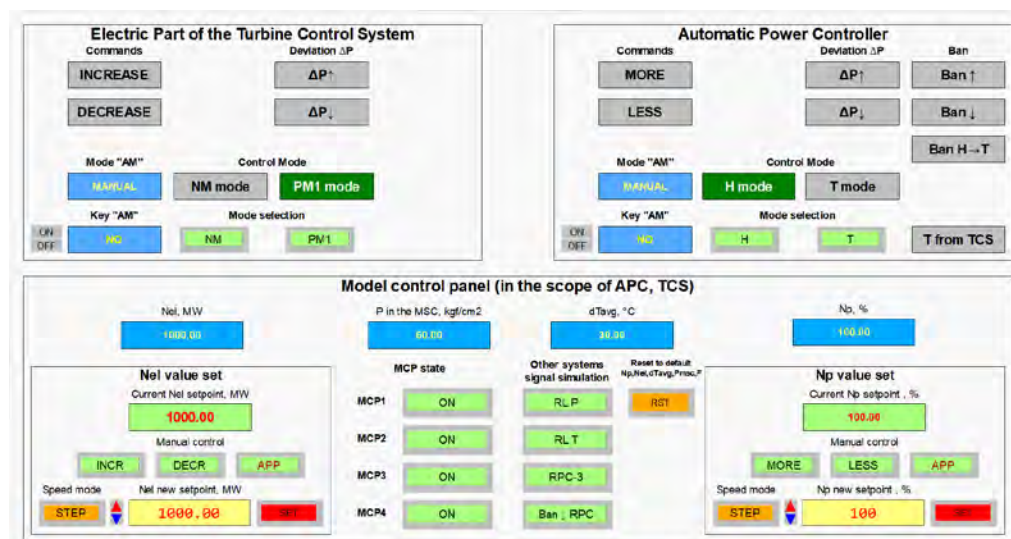
# RadICS Platform Overview. MATS

## Functions:

- Configuration delivery
- Acquiring Application Data from FSC(s)
- Archiving Application Data
- Providing data to Client Software
- Visualization data to Operator(s)
- Tuning FSC parameters

## Features:

- Multiuser network environment (LAN TCP/IP)



# RadICS Platform Overview. ROVT

## Compilation results review. ROVT checks:

- RPCT project build integrity,
- compilation log,
- LM resources consumption.

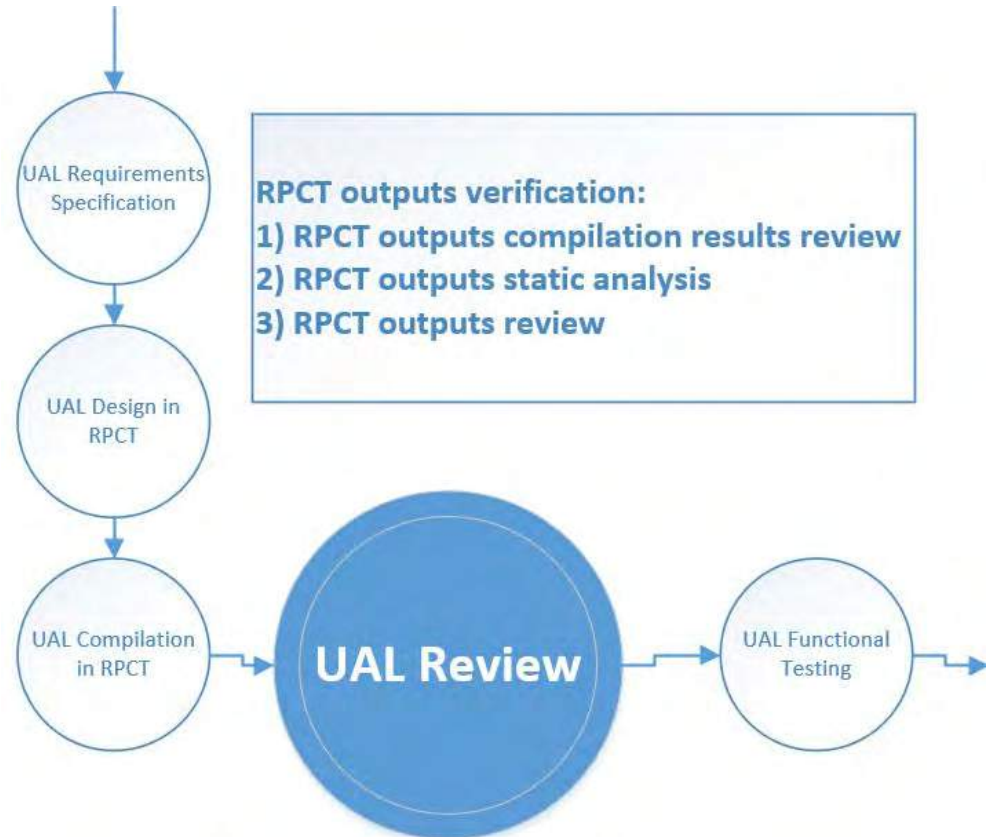
## Static analysis. ROVT performs a set of checks to ensure:

- integrity of bitstream file,
- correctness of LM's binary commands translation,
- correctness of UAL itself

## Review. ROVT generates a set of reverse-engineered reports on:

- RPCT project UAL components and connections,
- HW configuration and tuning signals.

Verifier has to compare design documentation with these reports and check if no discrepancies exists.



# RadICS Platform Overview. UAL Design Principles

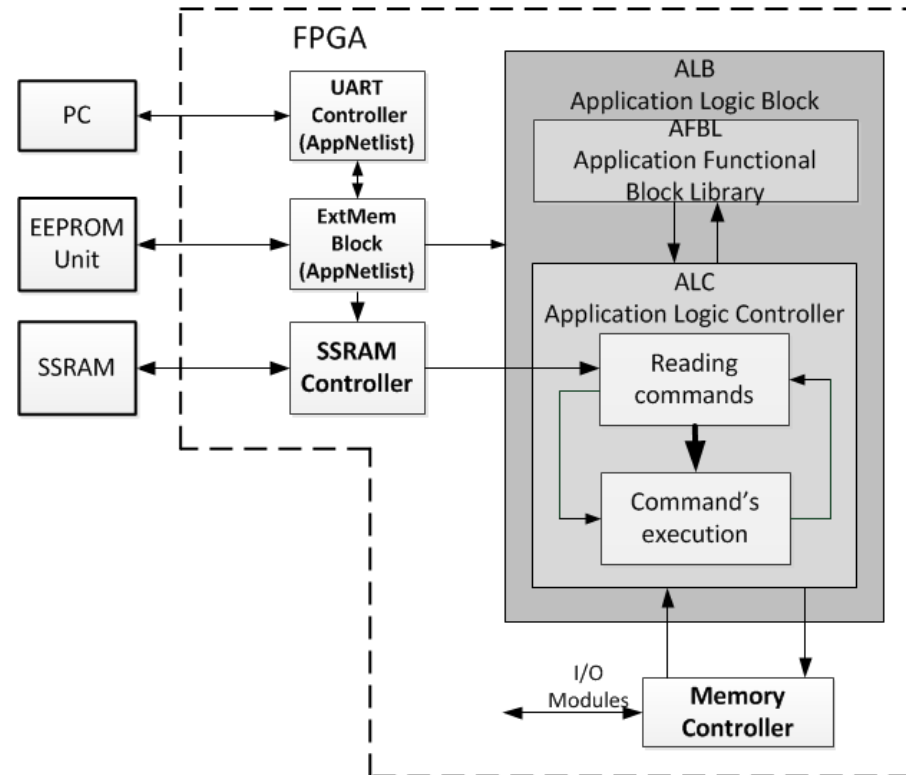
- Provide End-User with libraries for Application Design based on IEC 61131 list of components and our experience in Nuclear I&C systems development and supporting process;
- Application level receives all needed diagnostic information;
- Application Functional Block Library (AFBL) components perform defensive measures to protect the application from “bad data”;
- Each AFBL Component signals the “error” condition to the application via special pinouts and allow the End User decide what to do (safe state for the whole system or for the particular board, announcing etc.);



# RadICS Platform Overview. UAL Design flows

**1<sup>st</sup> Design Flow** - User Application Logic (UAL) is a part of FPGA-design. UAL-designer operates with AFBL components directly (Quartus II is used, reverse engineering projects only);

**2<sup>nd</sup> Design Flow** - UAL is a bitstream generated by RadICS Platform Configuration Toolset (RPCT), stored in the Logic Module external EEPROM and processed by special AFB Controller inside the LM module FPGA each work cycle. UAL-designer operates with AFBL components via RPCT;



# RadICS Platform Overview. AFB Controller

- **AFB Controller is FSM** which performs operations in accordance with UAL bitstream generated by RPCT and stored in external EEPROM;
- **AFB Controller doesn't have branches or cycles;**
- **AFB Controller doesn't have interruptions;**
- AFB Controller provides determined processing time;
- AFB Controller operates with determined redundant and physically separated sets of AFBL Components;
- AFB Controller is not able to modify UAL bitstream or any input data;
- AFB Controller performs self-diagnostics to detect possible failures (SEU and user errors);

# RadICS Platform based installations

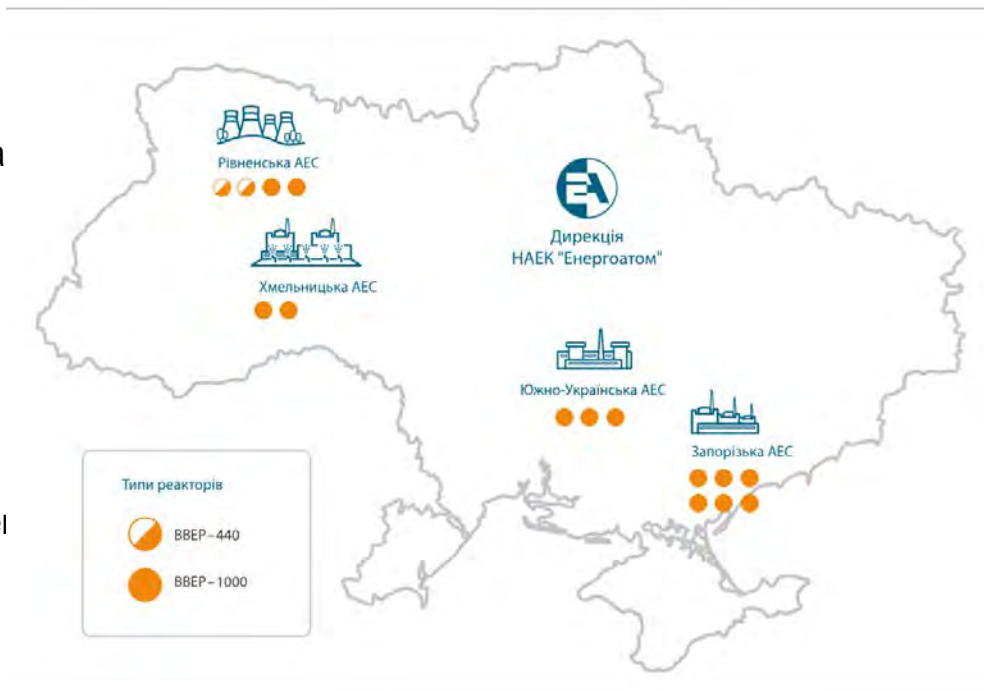
Starting from 2015 RPC Radiy installed 9 systems

## Quartus support (4 systems):

- Embalse NPP – Annunciation System
- RNPP (3<sup>rd</sup> unit) – Nuclear Island and Conventional Island I&C System,
- SUNPP (3<sup>rd</sup> unit) – RTS

## RPCT support (5 systems):

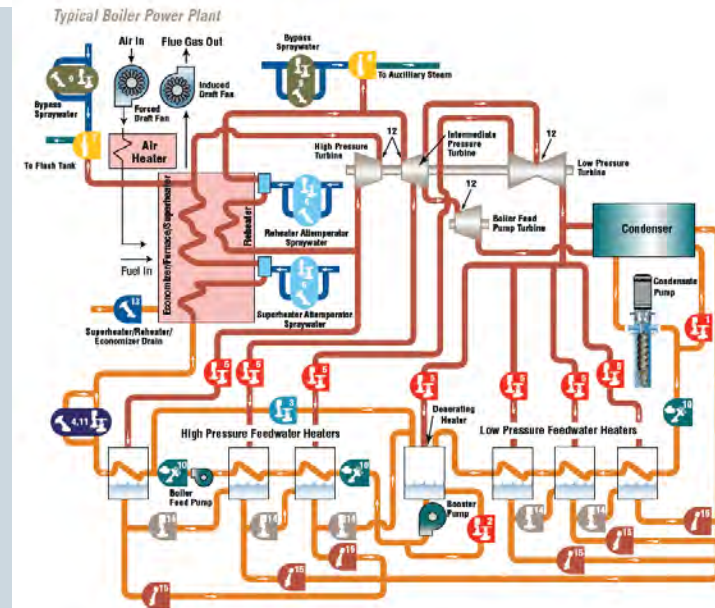
- RNPP (3<sup>rd</sup> unit) – SFAS
- KNPP (1<sup>st</sup> unit) – SFAS, Nuclear Island I&C System
- SUNPP (3<sup>rd</sup> unit) – SFAS, Nuclear Island I&C System



# Motivation

- To check if our equipment (both HW and support SW) are ready for high complexity projects implementation

# PID Controller implementation



# Object Description

Turbine automatic control and speed-up protection system (TCS) which is intended for (in normal and emergency modes of operation without operator intervention):

- Precise pressure and power regulation in accordance with defined static characteristic needed for the systems of frequency and active power secondary regulation.
- Automatic turbogenerator rotation frequency maintaining etc.



# Object Description

TCS consists of two parts – electric and hydraulic

Electric part is divided into slow and fast-acting loops of turbine control

In a slow-acting turbine control loop, impacts on the motor of the Turbine Control Mechanism (TCM) are formed to ensure normal (non-emergency) remote or automatic control of the turbine.

In accordance with a position of mode keyswitch in the main control room or in accordance with commands from automatic regulation devices there are several modes of operation. One of them is a mode of automatic pressure regulation before turbine (PM1 mode).

# Object Description. Regulation law. Pressure mode

In the pressure mode commands “Increase” or “Decrease” are generated to provide the movement of the turbine’s CV that is necessary to realize the regulation law in accordance with the formula:

$$Y = (P - P_0) + K_n \cdot T_n \cdot dN/dt + K_p \cdot T_p \cdot dP/dt,$$

where  $Y$  – control impact;

$K_p$  – pressure transfer ratio in MSH;

$K_n$  – electric power transfer ratio in the feedback loop;

$P$  – the current pressure’s value in MSH ;

$P_0$  – the setpoint value of pressure in MSH;

$T_n$  – derivative time constant of electrical power;

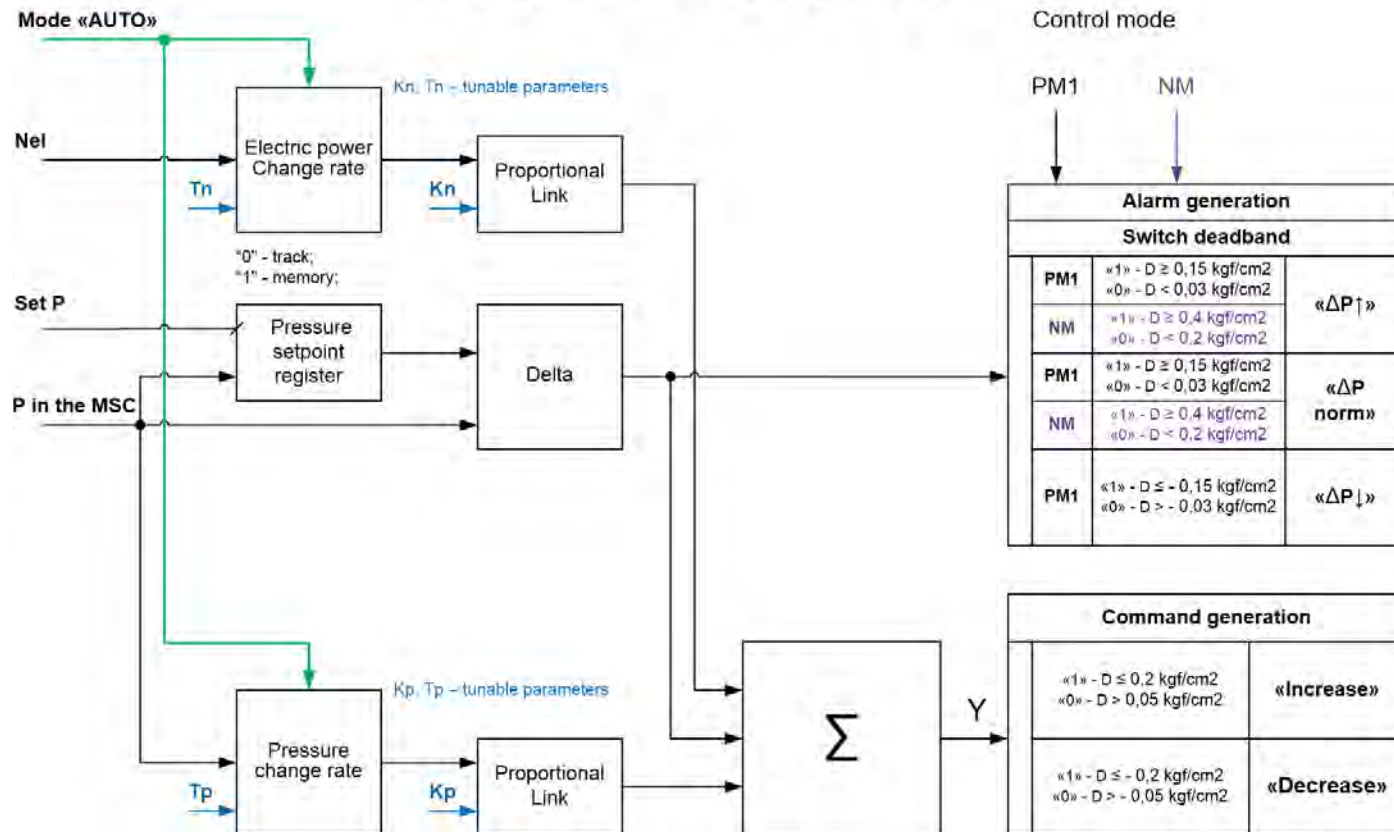
$T_p$  – derivative time constant of pressure in MSH.

\* MSH – main steam header; CV – control valve

# TCS Controller block diagram (PM1 mode)

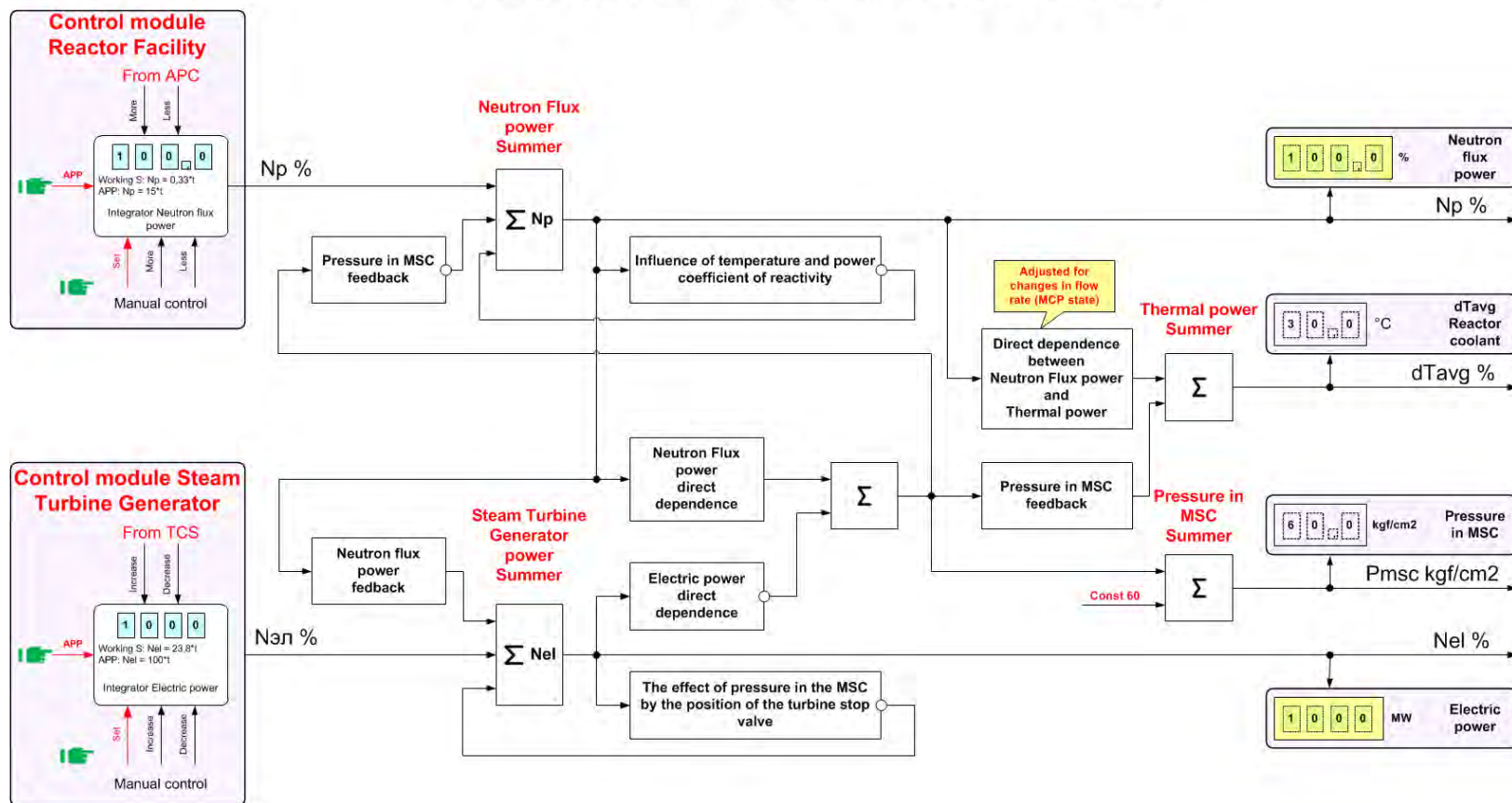
TCS controller block diagram (PM1 mode)

$$Y = (P - P_0) + K_n \cdot T_n \cdot dN/dt + K_p \cdot T_p \cdot dP/dt$$



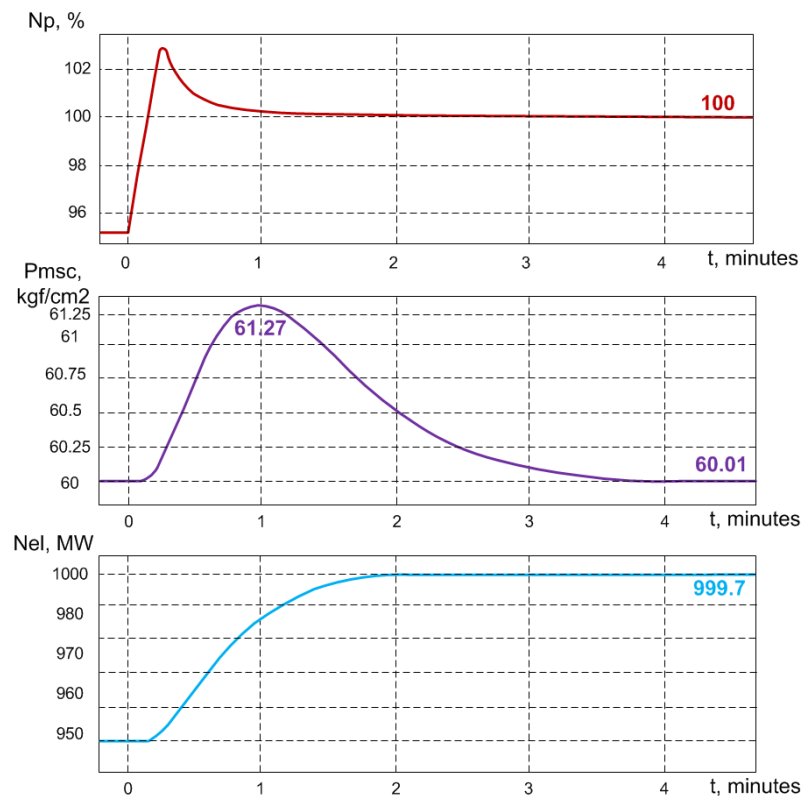
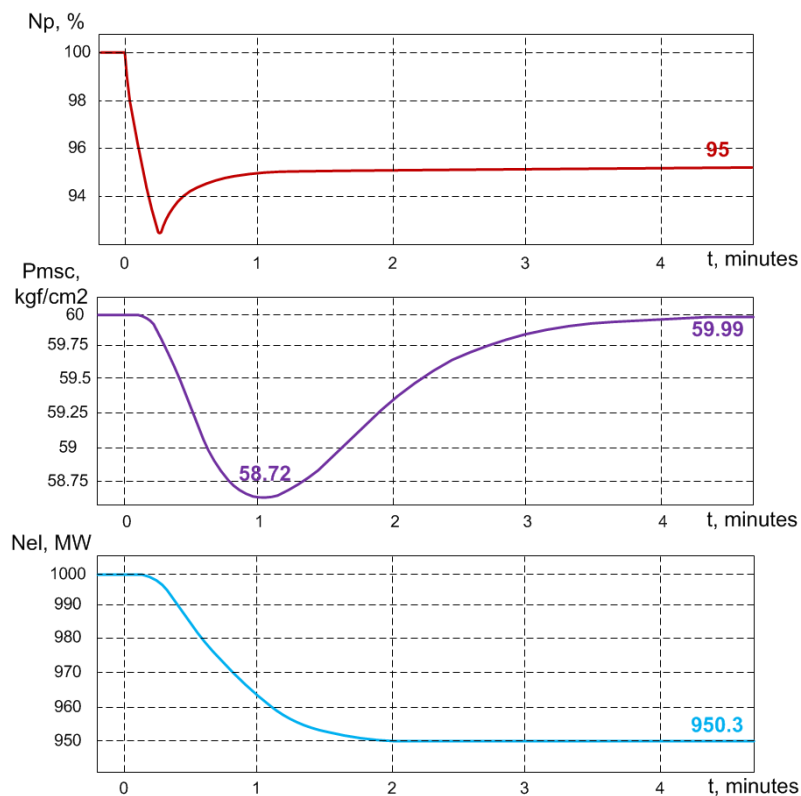
# Reactor Model

Reactor processes model (in the scope of APC, TCS)

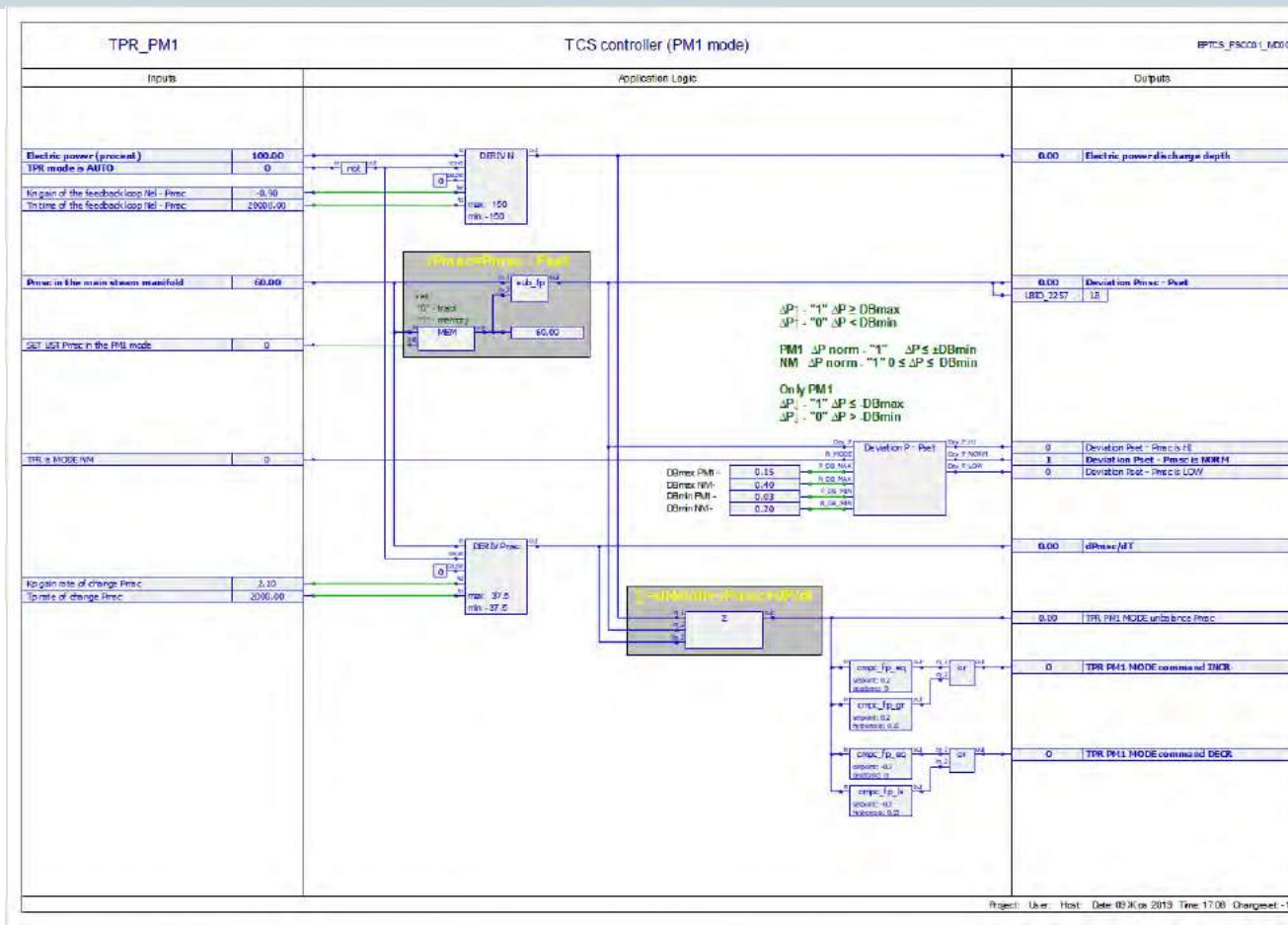


# Dynamic characteristics curves

Dynamic characteristics when disturbed by a control rod group (TCS controller is ON)

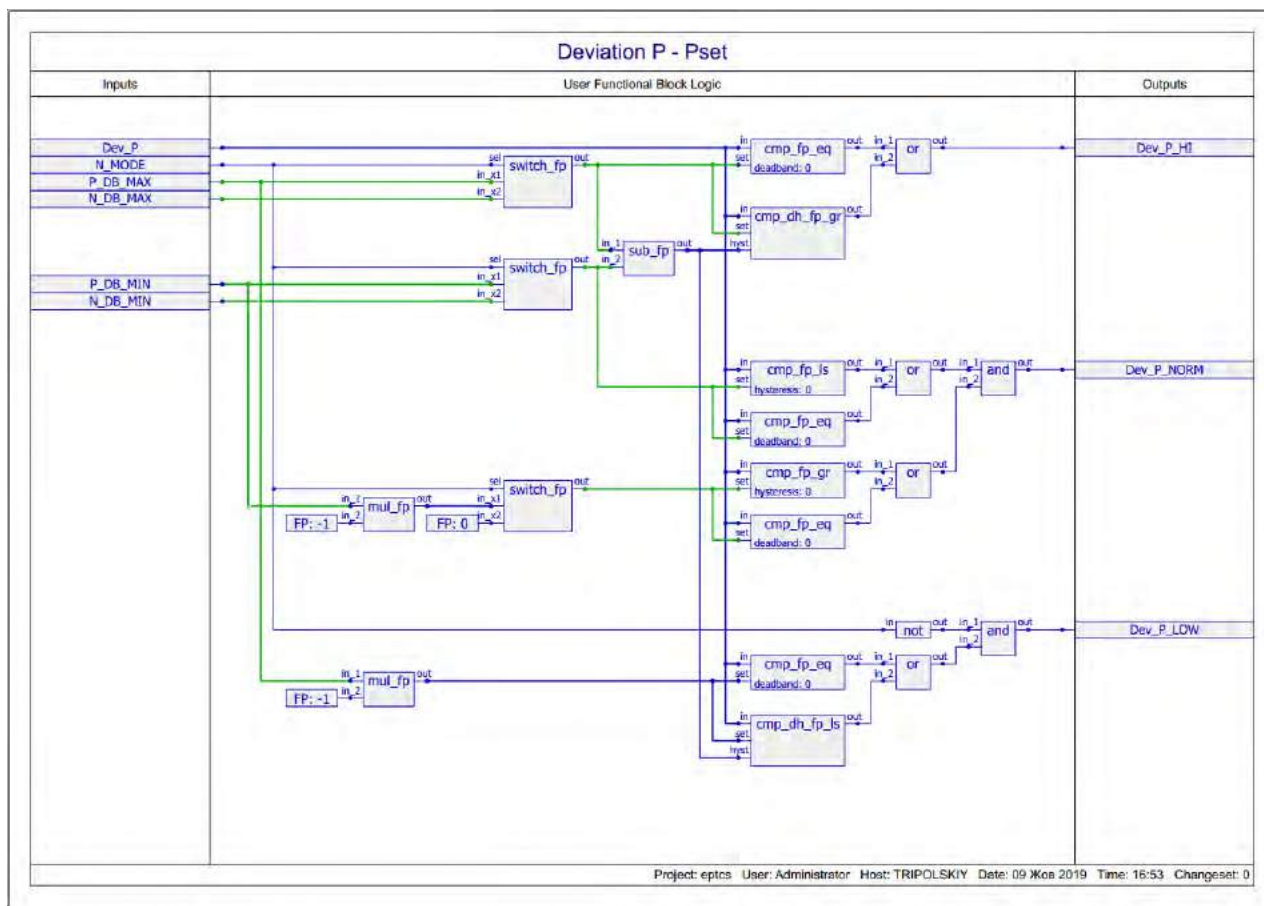


# Implementation. Regulator





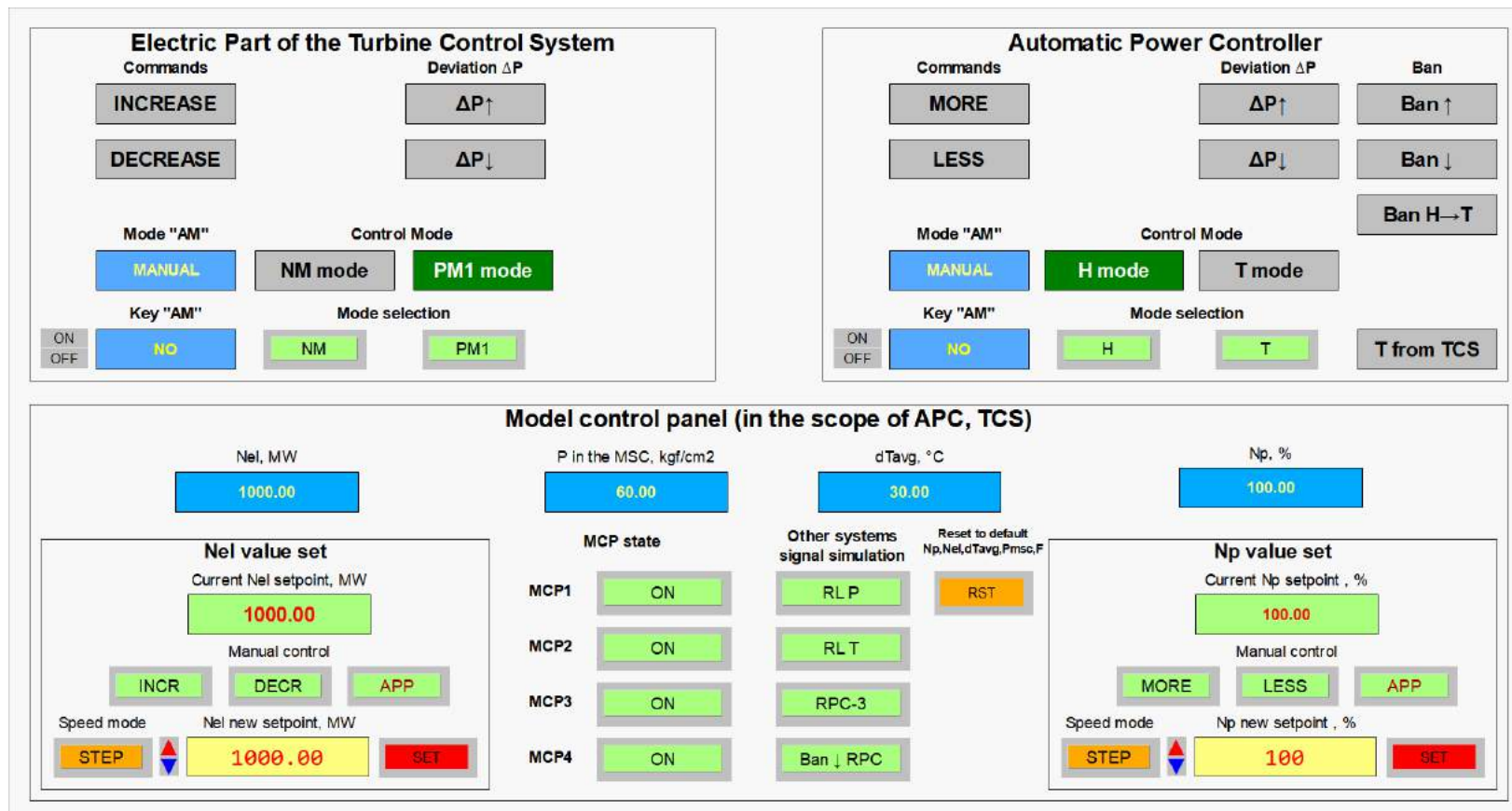
# Implementation. Regulator. UFB



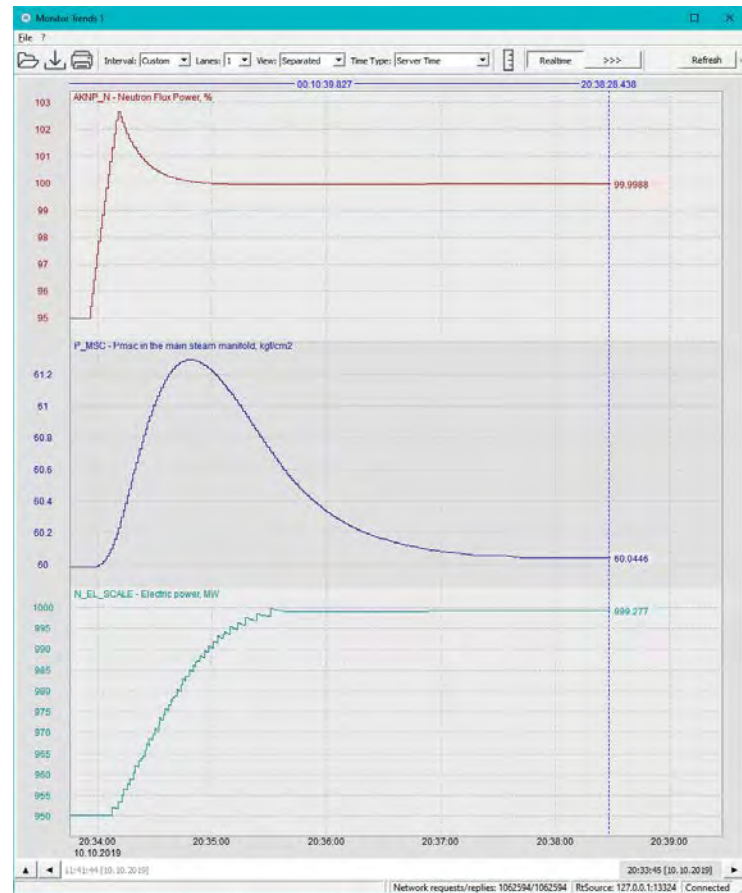
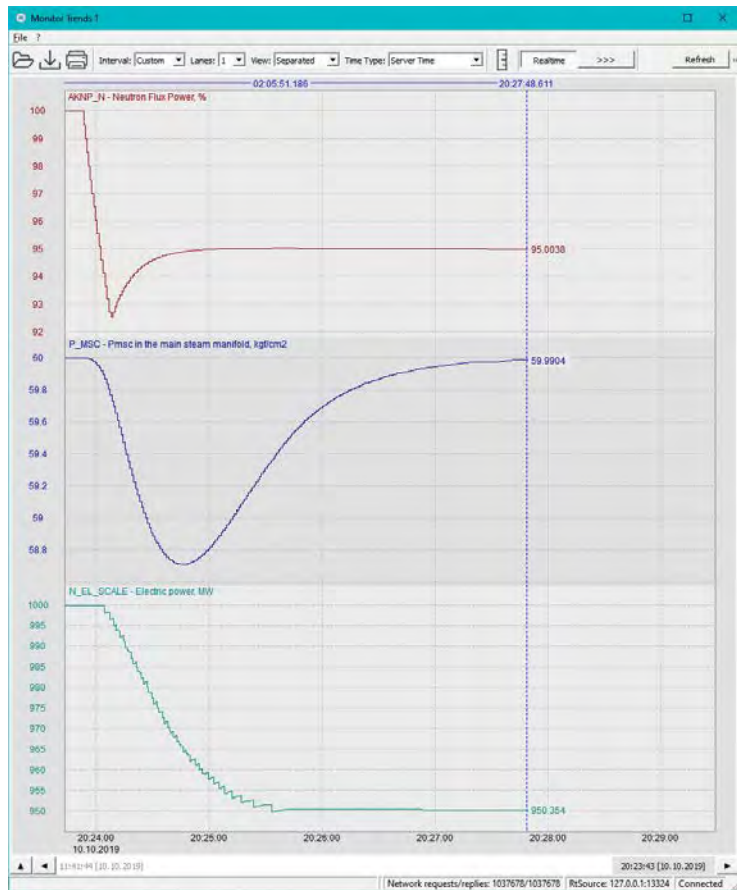
RPC Radiy



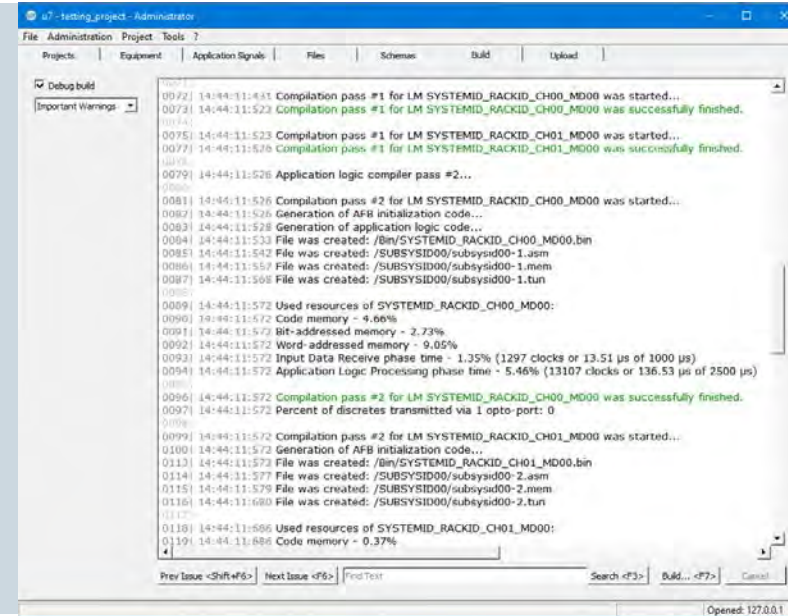
# Implementation. HMI



# Implementation. Graphs



# Implementation results



The screenshot shows the 'u7-testing\_project - Administrator' window. The 'Build' tab is selected, displaying a detailed log of the compilation process. The log includes timestamps and messages for various steps, such as compilation passes, file creation, and resource usage. The status bar at the bottom indicates 'Opened: 127.0.0.1'.

```
0072| 14:44:11:481 Compilation pass #1 for LM SYSTEMID_RACKID_CH00_MD00 was started...
0073| 14:44:11:523 Compilation pass #1 for LM SYSTEMID_RACKID_CH00_MD00 was successfully finished.
0074|
0075| 14:44:11:523 Compilation pass #1 for LM SYSTEMID_RACKID_CH01_MD00 was started...
0077| 14:44:11:526 Compilation pass #1 for LM SYSTEMID_RACKID_CH01_MD00 was successfully finished.
0078|
0079| 14:44:11:526 Application logic compiler pass #2...
0080|
0081| 14:44:11:526 Compilation pass #2 for LM SYSTEMID_RACKID_CH00_MD00 was started...
0082| 14:44:11:526 Generation of AFB initialization code...
0083| 14:44:11:528 Generation of application logic code...
0084| 14:44:11:533 File was created: /Bin/SYSTEMID_RACKID_CH00_MD00.bin
0085| 14:44:11:542 File was created: /SUBSYSID00/subsysid00-1.asm
0086| 14:44:11:557 File was created: /SUBSYSID00/subsysid00-1.mem
0087| 14:44:11:568 File was created: /SUBSYSID00/subsysid00-1.tun
0088|
0089| 14:44:11:572 Used resources of SYSTEMID_RACKID_CH00_MD00:
0090| 14:44:11:572 Code memory - 4.66%
0091| 14:44:11:572 Bit-addressed memory - 2.73%
0092| 14:44:11:572 Word-addressed memory - 9.05%
0093| 14:44:11:572 Input Data Receive phase time - 1.35% (1297 clocks or 13.51 µs of 1000 µs)
0094| 14:44:11:572 Application Logic Processing phase time - 5.46% (13107 clocks or 136.53 µs of 2500 µs)
0095|
0096| 14:44:11:572 Compilation pass #2 for LM SYSTEMID_RACKID_CH00_MD00 was successfully finished.
0097| 14:44:11:572 Percent of discretes transmitted via 1 opto-port: 0
0098|
0099| 14:44:11:572 Compilation pass #2 for LM SYSTEMID_RACKID_CH01_MD00 was started...
0100| 14:44:11:572 Generation of AFB initialization code...
0101| 14:44:11:573 File was created: /Bin/SYSTEMID_RACKID_CH01_MD00.bin
0102| 14:44:11:577 File was created: /SUBSYSID00/subsysid00-2.asm
0103| 14:44:11:579 File was created: /SUBSYSID00/subsysid00-2.mem
0104| 14:44:11:580 File was created: /SUBSYSID00/subsysid00-2.tun
0105|
0106| 14:44:11:586 Used resources of SYSTEMID_RACKID_CH01_MD00:
0107| 14:44:11:586 Code memory - 0.37%
```

# Application Logic Design Flows.

## Comparison Table

Two different approaches of UAL execution in the platform	
FPGA only (1 <sup>st</sup> Design Flow)	FPGA (Controller) + external EEPROM (Logic) (2 <sup>nd</sup> Design Flow)
Features	
Full parallelism is available	Only serial execution for application logic
UAL capacity depends on FPGA resources usage	UAL capacity depends on external EEPROM size
UAL change means FPGA ED recompilation	Frozen FPGA ED design.
FPGA vendor design tools are used to create and simulate UAL	RPCT
UAL V&V scope includes activities related to FPGA (LLS, STA, TS etc.)	UAL V&V process is simpler.
UAL designers have to be qualified in the field of HDL programming and be familiar with Logic Module ED architecture	Qualification requirements for designers are lower



# Fast Compilation

Plant Protection System RPCT project with dozens of Logic Modules requires not more than 5 minutes to be compiled.

4.5 hours to compile one LM FPGA project

Tasks		
Flow: <span>Compilation</span> <span>Customize...</span>		
Task	Time	
✓  Compile Design	04:28:14	
✓  ▶ Analysis & Synthesis	00:52:51	
✓  ▶ Fitter (Place & Route)	03:00:55	
✓  ▶ Assembler (Generate programming files)	00:13:49	
✓  ▶ TimeQuest Timing Analysis	00:08:27	
✓  ▶ EDA Netlist Writer	00:04:44	
Program Device (Open Programmer)		

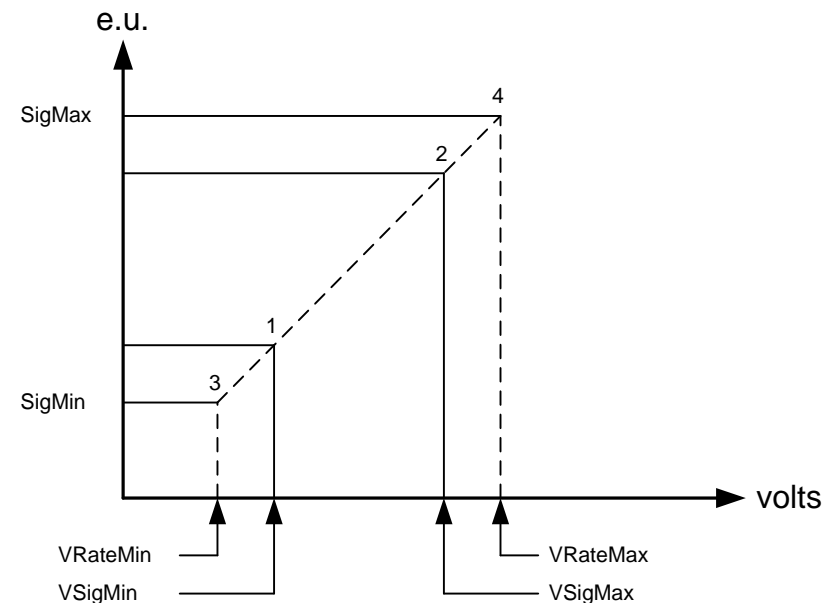
```
0071 14:44:11:431 Compilation pass #1 for LM SYSTEMID_RACKID_CH00_MD00 was started...
0072 14:44:11:523 Compilation pass #1 for LM SYSTEMID_RACKID_CH00_MD00 was successfully finished.
0074
0075 14:44:11:523 Compilation pass #1 for LM SYSTEMID_RACKID_CH01_MD00 was started...
0077 14:44:11:526 Compilation pass #1 for LM SYSTEMID_RACKID_CH01_MD00 was successfully finished.
0078
0079 14:44:11:526 Application logic compiler pass #2...
0080
0081 14:44:11:526 Compilation pass #2 for LM SYSTEMID_RACKID_CH00_MD00 was started...
0082 14:44:11:526 Generation of AFB initialization code...
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0084 14:44:11:533 File was created: /Bin/SYSTEMID_RACKID_CH00_MD00.bin
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0086 14:44:11:557 File was created: /SUBSYSID00/subsysid00-1.mem
0087 14:44:11:568 File was created: /SUBSYSID00/subsysid00-1.tun
0088
0089 14:44:11:572 Used resources of SYSTEMID_RACKID_CH00_MD00:
0090 14:44:11:572 Code memory - 4.66%
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0092 14:44:11:572 Word-addressed memory - 9.05%
0093 14:44:11:572 Input Data Receive phase time - 1.35% (1297 clocks or 13.51 µs of 1000 µs)
0094 14:44:11:572 Application Logic Processing phase time - 5.46% (13107 clocks or 136.53 µs of 2500 µs)
0095
0096 14:44:11:572 Compilation pass #2 for LM SYSTEMID_RACKID_CH00_MD00 was successfully finished.
0097 14:44:11:572 Percent of discretes transmitted via 1 opto-port: 0
0098
0099 14:44:11:572 Compilation pass #2 for LM SYSTEMID_RACKID_CH01_MD00 was started...
0100 14:44:11:572 Generation of AFB initialization code...
0113 14:44:11:573 File was created: /Bin/SYSTEMID_RACKID_CH01_MD00.bin
0114 14:44:11:577 File was created: /SUBSYSID00/subsysid00-2.asm
0115 14:44:11:579 File was created: /SUBSYSID00/subsysid00-2.mem
0116 14:44:11:680 File was created: /SUBSYSID00/subsysid00-2.tun
0117
0118 14:44:11:686 Used resources of SYSTEMID_RACKID_CH01_MD00:
0119 14:44:11:686 Code memory - 0.37%
```

5 minutes to compile whole system

# Design UAL in Engineering Units

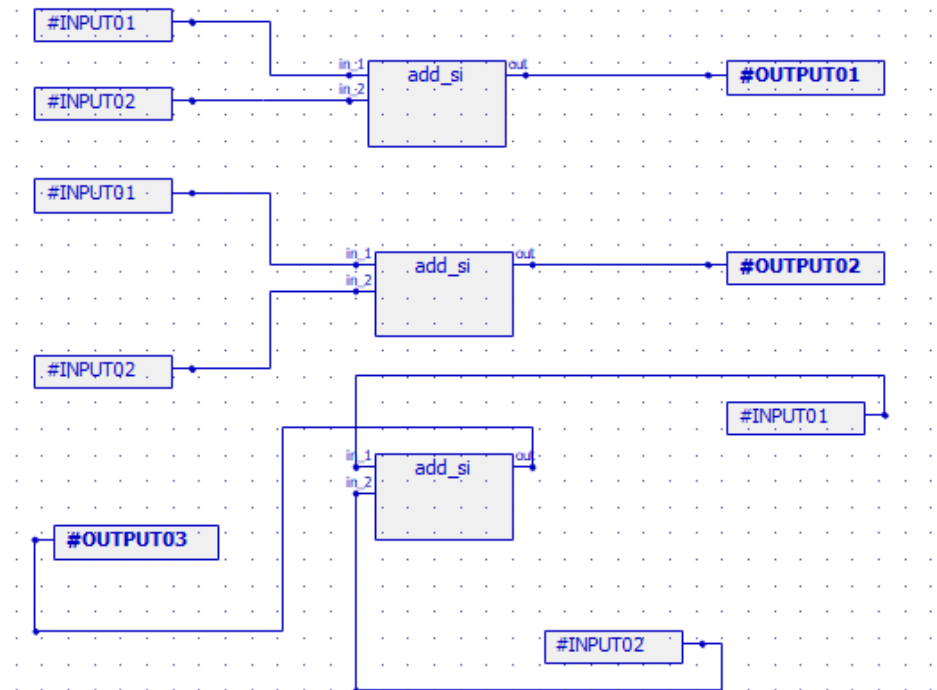
## Behind the scenes conversion of analog signals to / from engineering units.

4 Signal processing	
ExcludeFromBuild	<input type="checkbox"/> False
FilteringTime	0.00000
HighEngineeringUnits	100.00
HighValidRange	100.00
LowEngineeringUnits	0.00
LowValidRange	0.00
SpreadTolerance	2.00000
Unit	
5 Electric parameters	
ElectricHighLimit	10.0000
ElectricLowLimit	-10.0000
ElectricUnit	V
SensorType	Minus10_Plus10_V



# Order of AFBs Execution

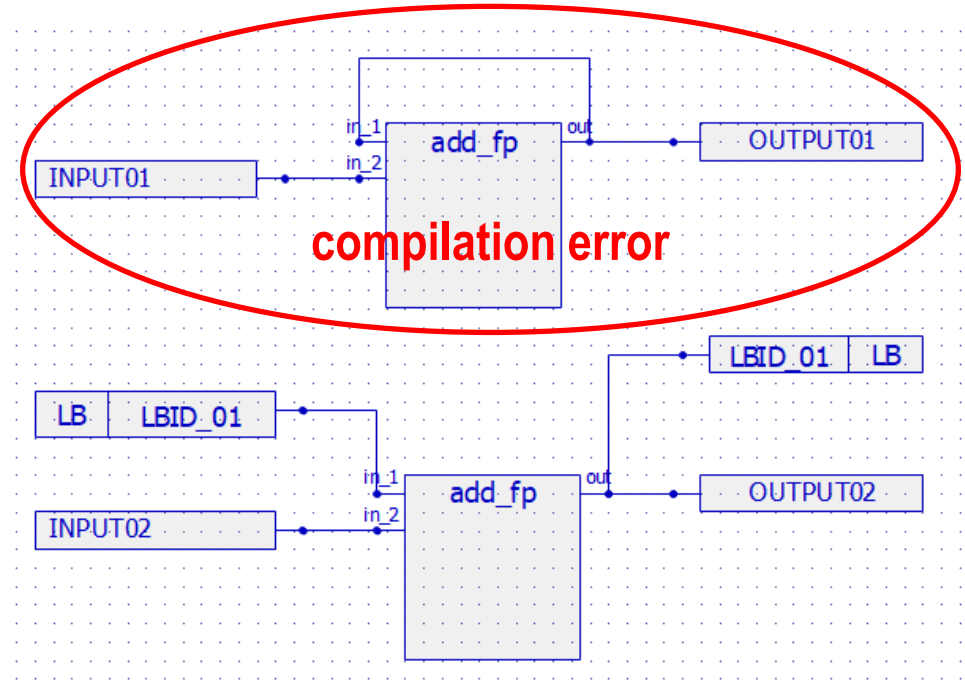
RPCT defines a logically correct execution order regardless of AFBs positions within UAL Schema.



**OUTPUT01 = OUTPUT02 = OUTPUT03**

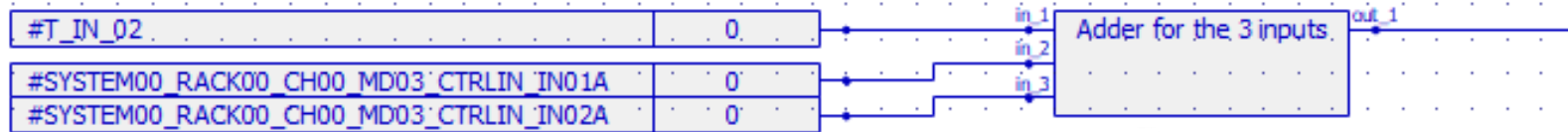
# Loopbacks Processing

- RPCT identifies loopbacks in UAL project and forms a compilation error
- If loopback is really necessary the dedicated elements Loopback Source / Target shall be used



# User Functional Block (UFB Schema)

- Predeveloped component
- Designed from AFBs only



Adder for the 3 inputs

User Functional Block Logic



# Short Work Cycle

LM's resources usage					
LM Equipment ID	Bit Memory, %	Word Memory, %	Code memory, %	IdrPhase Time, %	AlpPhase Time, %
!! SFIT_RACKID_CH01_MD00	30.08	76.19	74.38	60.31	99.98

FSC work cycle ("scan time") is 5 ms.

During this time the single Logic Module is able to implement up to 256 PID Controllers plus 256 Low Pass Filters.

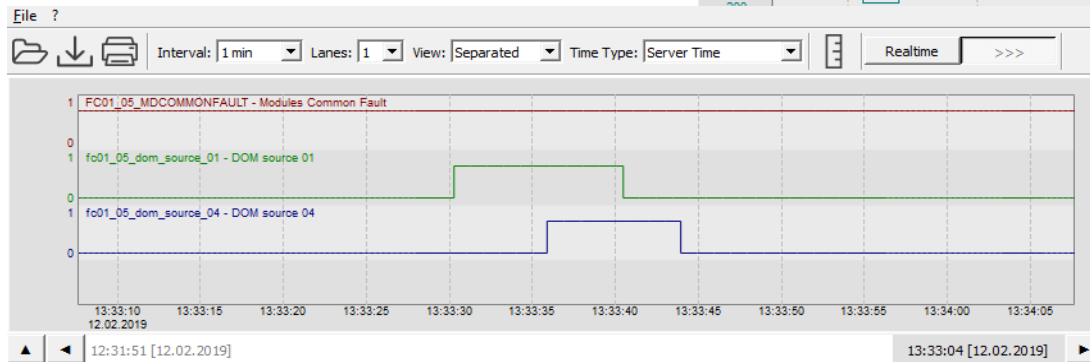
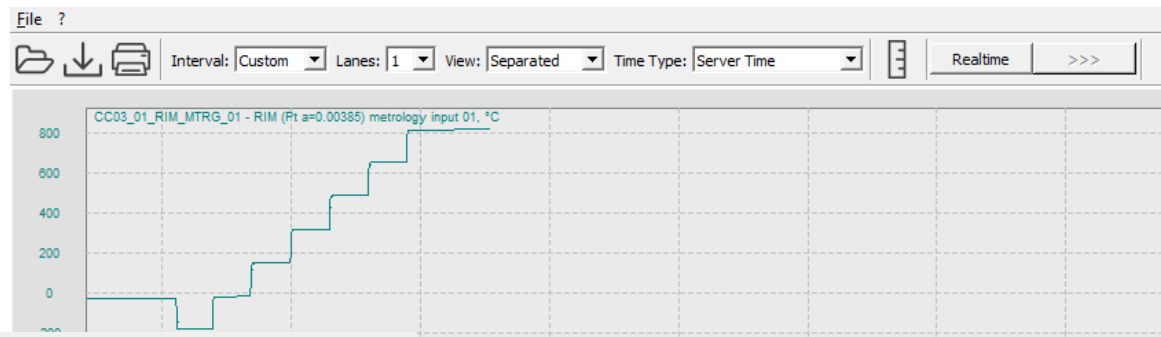
LM SFIT_RACKID_CH01_MD00 AFB components usage						
	OpCode	Caption	UsagePercent	UsedInstances	MaxInstances	Version
	1	LOGIC	2.34	6	256	206
	2	NOT	0.00	0	1	103
	3	TCT	0.00	0	256	207
	4	FLIP_FLOP	0.00	0	256	106
	5	CTUD	2.34	6	256	106
	6	MAJ	3.13	8	256	106
	7	SRSST	0.00	0	1	104
	8	BCOD	0.00	0	256	103
	9	BDEC	0.00	0	256	103
	10	BCOMP	0.00	0	256	110
!!	11	DAMPER	100.00	256	256	111
	13	MATH	0.78	2	256	104
	14	SCALE	1.56	4	256	107
	16	FUNC	0.00	0	256	1
!!	17	INT	100.00	256	256	5
	20	DPCOMP	39.06	98	256	3
	21	MUX	0.00	0	1	1
!!	22	LATCH	100.00	256	256	3
	23	LIM	0.00	0	256	7
	25	POL	0.00	0	256	3
!!	26	DER	100.00	256	256	4
	27	MISMATCH	0.00	0	256	1
	28	TCONV	0.00	0	256	0



# Precise Signal Analyzing

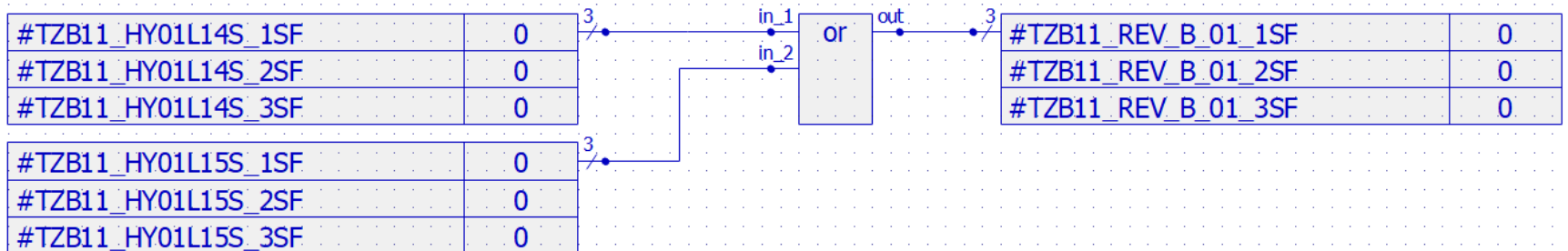
Plant time stamp follows to each signal acquired by MATS.

This allows to analyze plant signals with 5 ms precision.



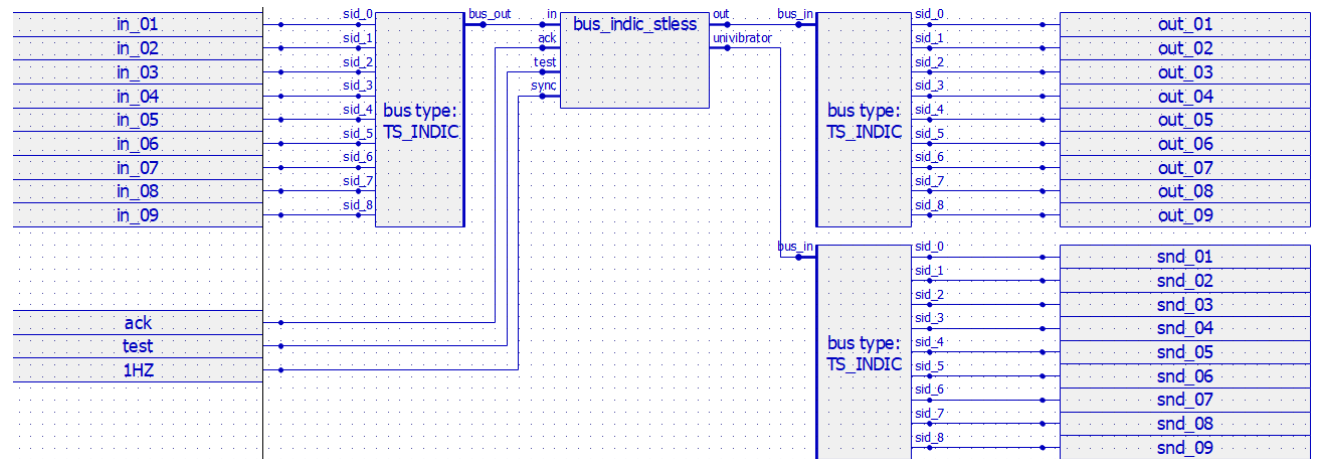
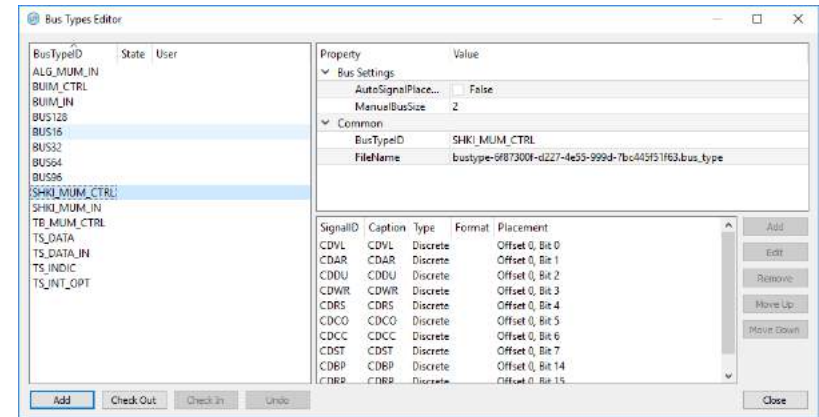
# Multi-channel Logic Schemas

- Schema can be bound to several logic modules
- Multi-channel signals and links
- Multi-channel AFB elements



# Buses

- Signals could be combined into buses
- Each bus has a customizable structure
- Bus Composer and Bus Extractor are used to combine/extract bus signals within a schema
- Specific AFB elements are used for buses processing



# Platform State Interfaces

The UAL can use a lot of diagnostic signals of the platform:

- Module temperature
- Module operating mode (STARTUP, RUN, RUN(SAFE), FAULTED, etc.)
- SOR and SOR Unit inputs states
- The validity of I/O signals

MD04_CTRLOUT_OUT32	A	Output
MD04_CTRLOUT_OUT32VALID	D	Input
MD04_PI_MODECONFIG	D	Input
MD04_PI_MODEFAULTED	D	Input
MD04_PI_MODEPOWEROFF	D	Input
MD04_PI_MODERUN	D	Input
MD04_PI_MODERUNSAFE	D	Input
MD04_PI_MODESTARTUP	D	Input
MD04_PI_SERIALNO	A	Input
MD04_PI_SORISSET	D	Input
MD04_PI_SORSWITCH1	D	Input
MD04_PI_SORSWITCH2	D	Input
MD04_PI_SORSWITCH3	D	Input
MD04_PI_TEMP	A	Input

# Conclusions

- RPCT is much easier and convenient for UAL design then Quartus II especially in system by system modernization
- RPCT results are easy verifiable (ROVT, but can be done by other organization, cause the outputs are easily readable)
- RadICS Platform (HW+ support SW) is ready to implement complex projects

# Thank you for your attention!

Research & Production Corporation Radiy  
29, Geroyiv Stalingrada Street, Kirovograd 25006, Ukraine  
e-mail: [ksleontiev@radiy.com](mailto:ksleontiev@radiy.com)  
<http://www.radiy.com>

