

# RadICS Platform Configuration Toolset (RPCT): Integrated Development Environment for FPGA-based Applications

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12 FPGA WS, October 14-16, 2019, Budapest, Hungary



# Agenda

- Introduction
- RPCT IDE Overview
- I&C Application Design Workflow
- Conclusions

# Introduction (what's new since Last meeting)

- Most Certified in the World I&C Platform RadICS
- IEC 61508:2010 compliant. Proved SIL 3 level in a single channel ([https://www.exida.com/2019/RAD\\_14-06-037\\_C001\\_V3R0\\_61508\\_Certificate\\_-\\_FSC.pdf](https://www.exida.com/2019/RAD_14-06-037_C001_V3R0_61508_Certificate_-_FSC.pdf))
- NRC approved for the use in safety related I&C systems in the USA (<https://www.nrc.gov/docs/ML1913/ML19134A193.pdf>)





# Certificate / Certificat Zertifikat / 合格証

RAD 1406037 C001

exida hereby confirms that the:

## FPGA-Based Safety Controller (FSC) RadICS

### RPC Radiy

29 Geroyiv Stalingrada Street  
Kirovograd, Ukraine

Has been assessed per the relevant requirements of:

**IEC 61508 : 2010 Parts 1-7**

and meets requirements providing a level of integrity to:

**Systematic Capability: SC 3 (SIL 3 Capable)**

**Random Capability: Type B Element**

**SIL 3 @ HFT=0; Route 1<sub>H</sub>**

**PFD<sub>AVG</sub>, PFH and Architecture Constraints  
must be verified for each application**

#### Safety Function:

The FSC will read input signals, perform user-defined application layer logic and write results to the output signals within the stated response time.

#### Application Restrictions:

The unit must be properly designed into a Safety Instrumented Function per the Safety Manual requirements.



*David Stattel*  
Evaluating Assessor

*Rudolf P. Chalupa*  
Certifying Assessor

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U.S. Nuclear Regulatory Commission Staff

Safety Evaluation for

Topical Report 2016-RPC003-TR-001

RadICS Safety System Digital Platform



Date: August 2019

Principal Contributors: Richard Stattel  
Dinesh Taneja

Enclosure

The manufacturer  
may use the mark:



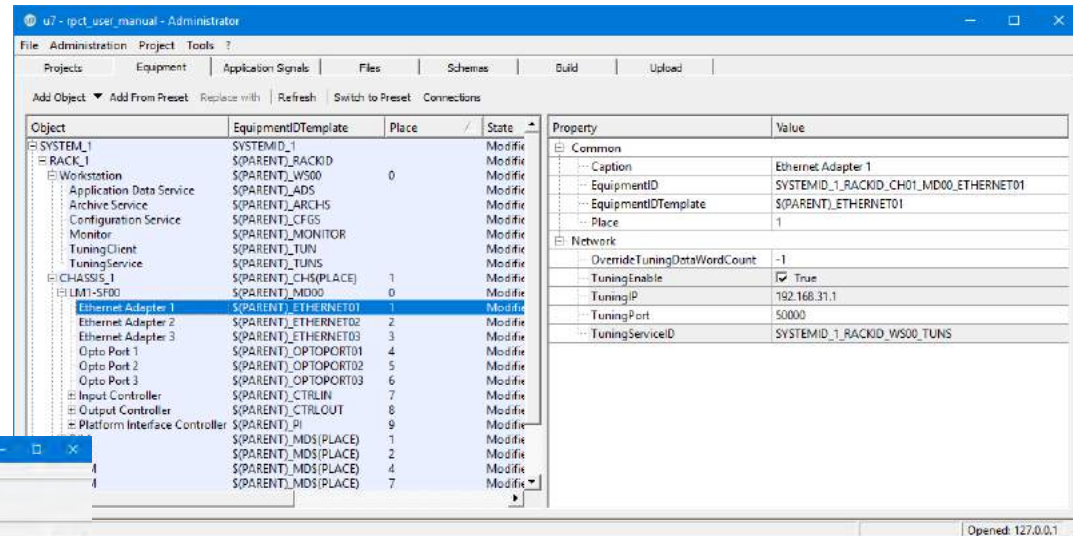
Revision 3.0 January 31, 2019  
Surveillance Audit Due  
February 1, 2022.



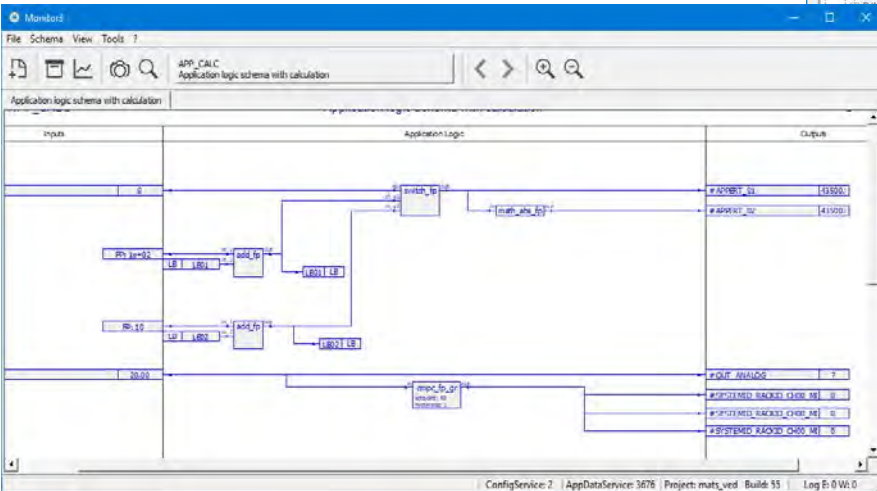
ISO/IEC 17020  
PRODUCT CERTIFICATION BODY  
#14000

# Software Overview

→ RPCT Integrated Development Environment (IDE)



→ Monitoring and Tuning System (MATS)



# RPCT Integrated Development Environment (IDE)

## Functions:

- Configure hardware architecture of I&C application
- Configure inter-optic connections
- Define Application Signals which will be used in User Application

## Logic

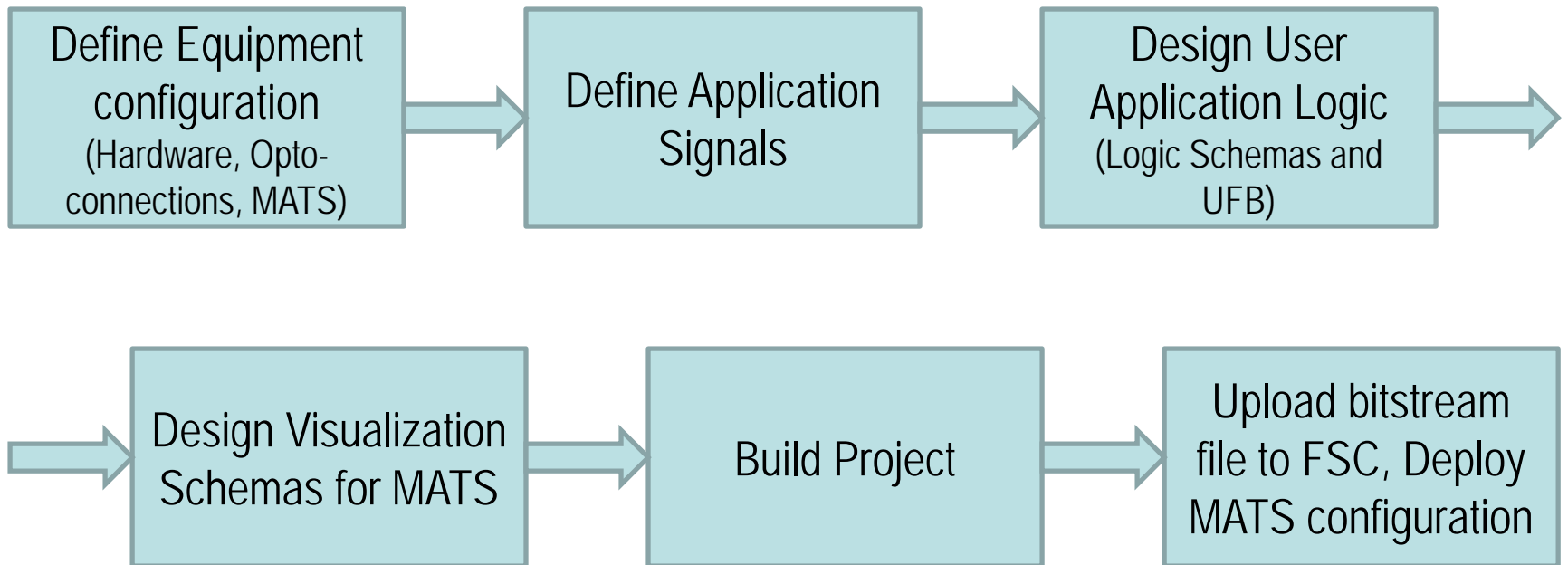
- Design User Application Logic (UAL)
- Configure MATS software
- Perform build, generate configuration files
- Upload bitstream file to the RadICS Platform

## Features:

- Multiuser access to project database
- Configuration Management

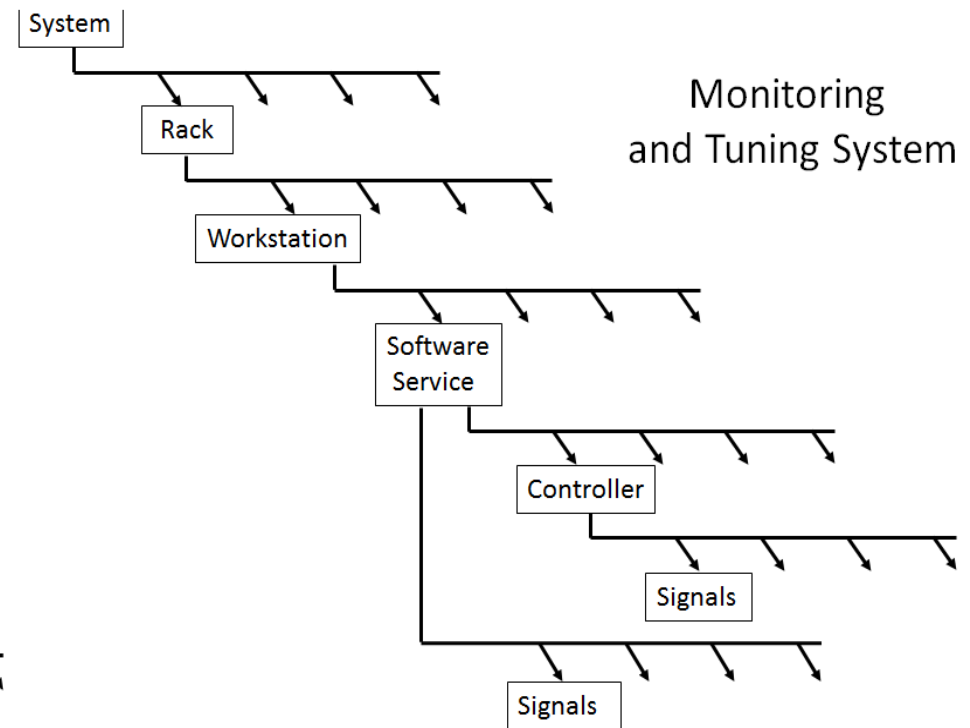
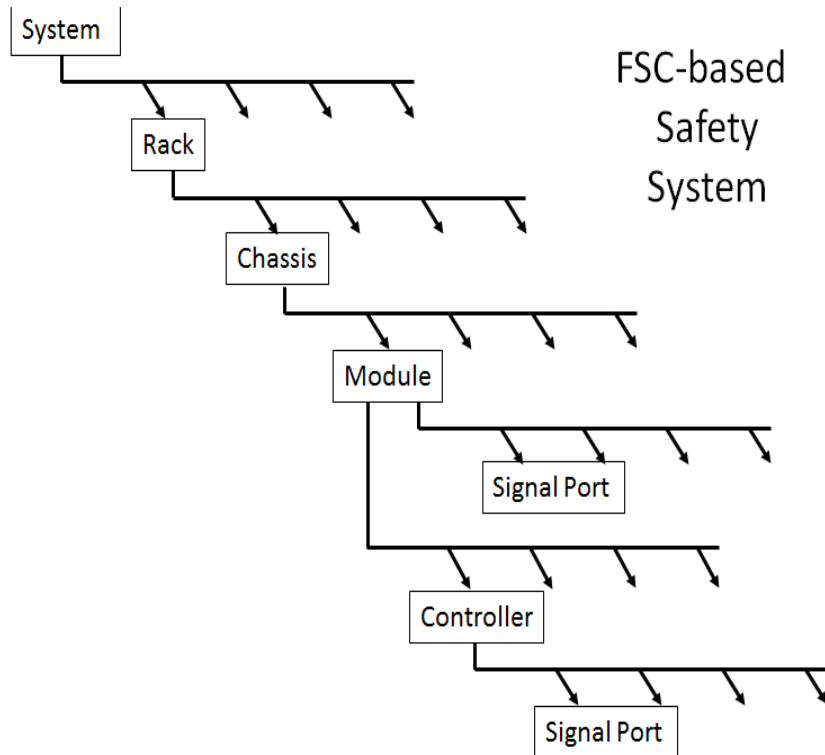
# RPCT Integrated Development Environment (IDE)

## Project Design workflow:



# RPCT Integrated Development Environment (IDE)

## Define I&C configuration (HW and MATS)

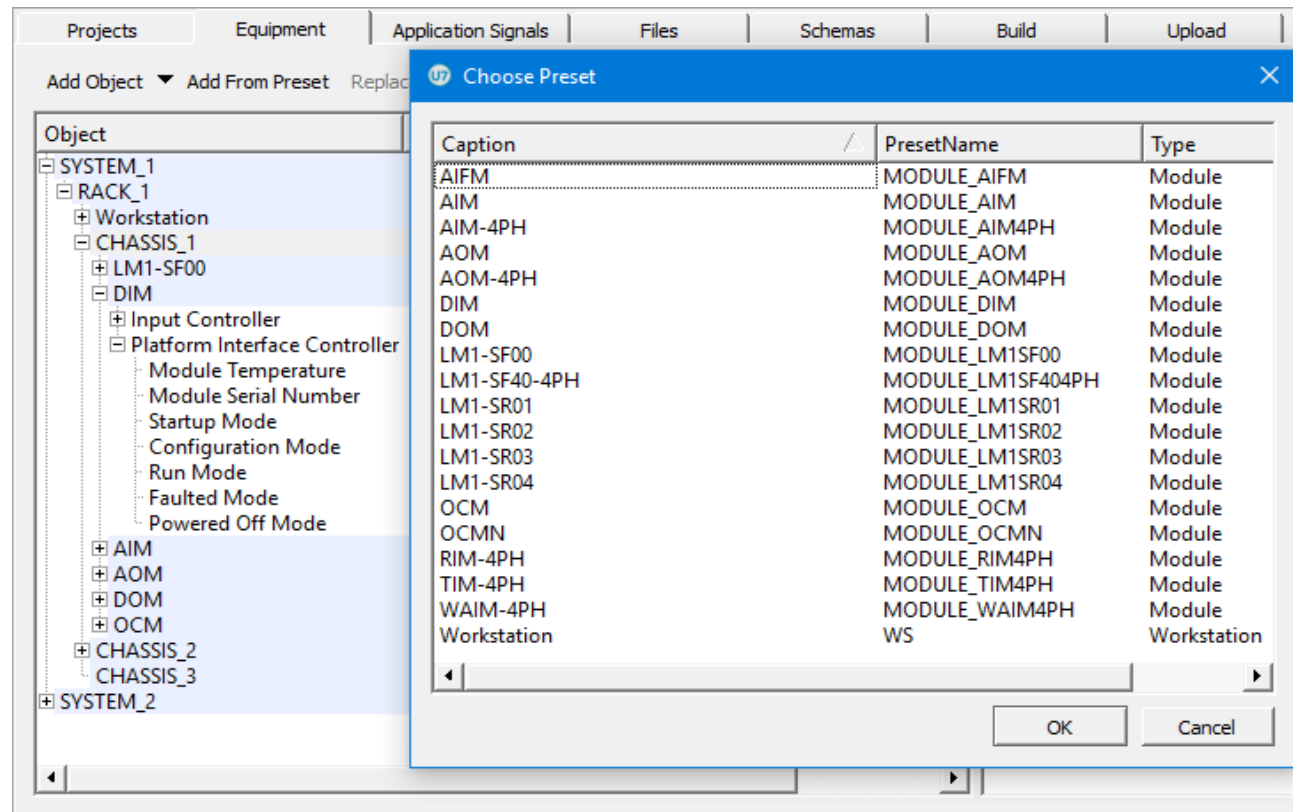




# RPCT Integrated Development Environment (IDE)

## Equipment hardware objects

- System
- Rack
- Chassis
- Modules (presets)
- Controller



# RPCT Integrated Development Environment (IDE)

## Equipment MATS objects

- Workstation
- Software (presets)
  - Configuration Service
  - Application Data Service
  - Tuning Service
  - Archive Service
  - Monitor
  - Tuning Client

The screenshot displays the RPCT IDE interface with the 'Equipment' tab selected. A table lists various MATS objects and their configurations. A 'Choose Preset' dialog box is open, showing a list of available presets.

Object	EquipmentIDTemplate	Place /	State
SYSTEM_1	SYSTEMID_1		Modified
RACK_1	\$(PARENT)_RACKID		Modified
Workstation	\$(PARENT)_WS00	0	Modified
Application Data Service	\$(PARENT)_ADS		Modified
Archive Service	\$(PARENT)_ARCHS		Modified
Configuration Service	\$(PARENT)_CFGS		Modified
Monitor	\$(PARENT)_MONITOR		Modified
TuningClient	\$(PARENT)_TUN		Modified
TuningService	\$(PARENT)_TUNS		Modified

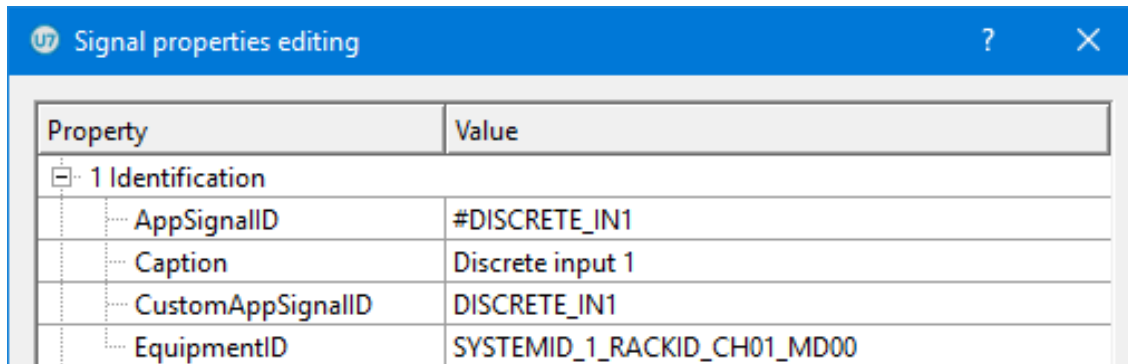
  

Caption	PresetName	Type
Application Data Service	ADS	Software
Archive Service	ARCHS	Software
Configuration Service	CFGS	Software
Diagnostics Data Service	DDS	Software
Metrology	METROLOGY	Software
Monitor	MONITOR	Software
TestClient	TESTCLIENT	Software
TuningClient	TUN	Software
TuningService	TUNS	Software

# RPCT Integrated Development Environment (IDE)

## Application Signals identification

- Application Signal ID (unique signal identifier for the whole project)
- Caption (Text description (purpose) of the signal)
- Custom Application Signal ID (Alternative signal identifier used in MATS)
- Equipment ID (Logic Module ID or hardware Signal Port ID)



Property	Value
1 Identification	
AppSignalID	#DISCRETE_IN1
Caption	Discrete input 1
CustomAppSignalID	DISCRETE_IN1
EquipmentID	SYSTEMID_1_RACKID_CH01_MD00

# RPCT Integrated Development Environment (IDE)

## Application Signals Types

### Analog Signals

- Input, Output, Internal
- Float or Signed Integer (32-bits)

2 Signal type	
InOutType	Input
Type	Analog
3 Data Format	
AnalogSignalFormat	Float32
ByteOrder	BigEndian
DataSize	32

### Discrete Signals

- Input, Output, Internal
- (1 bit)

2 Signal type	
InOutType	Input
Type	Discrete
3 Data Format	
ByteOrder	BigEndian
DataSize	1

### Bus Signals

- Internal
- Bus

2 Signal type	
InOutType	Internal
Type	Bus

# RPCT Integrated Development Environment (IDE)

Design UAL in engineering units

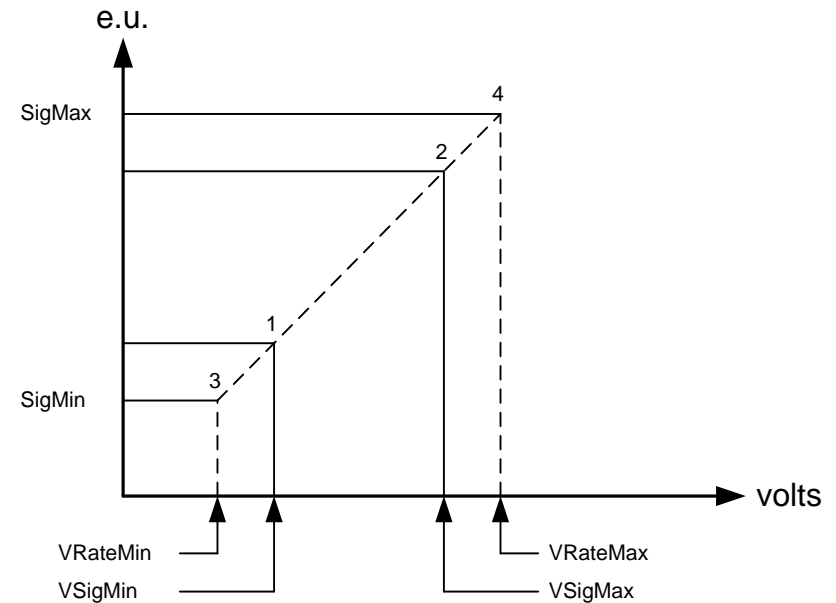
Behind the scenes conversion  
analog signals to / from  
engineering units.

## 4 Signal processing

ExcludeFromBuild	<input type="checkbox"/> False
FilteringTime	0.00000
HighEngineeringUnits	100.00
HighValidRange	100.00
LowEngineeringUnits	0.00
LowValidRange	0.00
SpreadTolerance	2.00000
Unit	

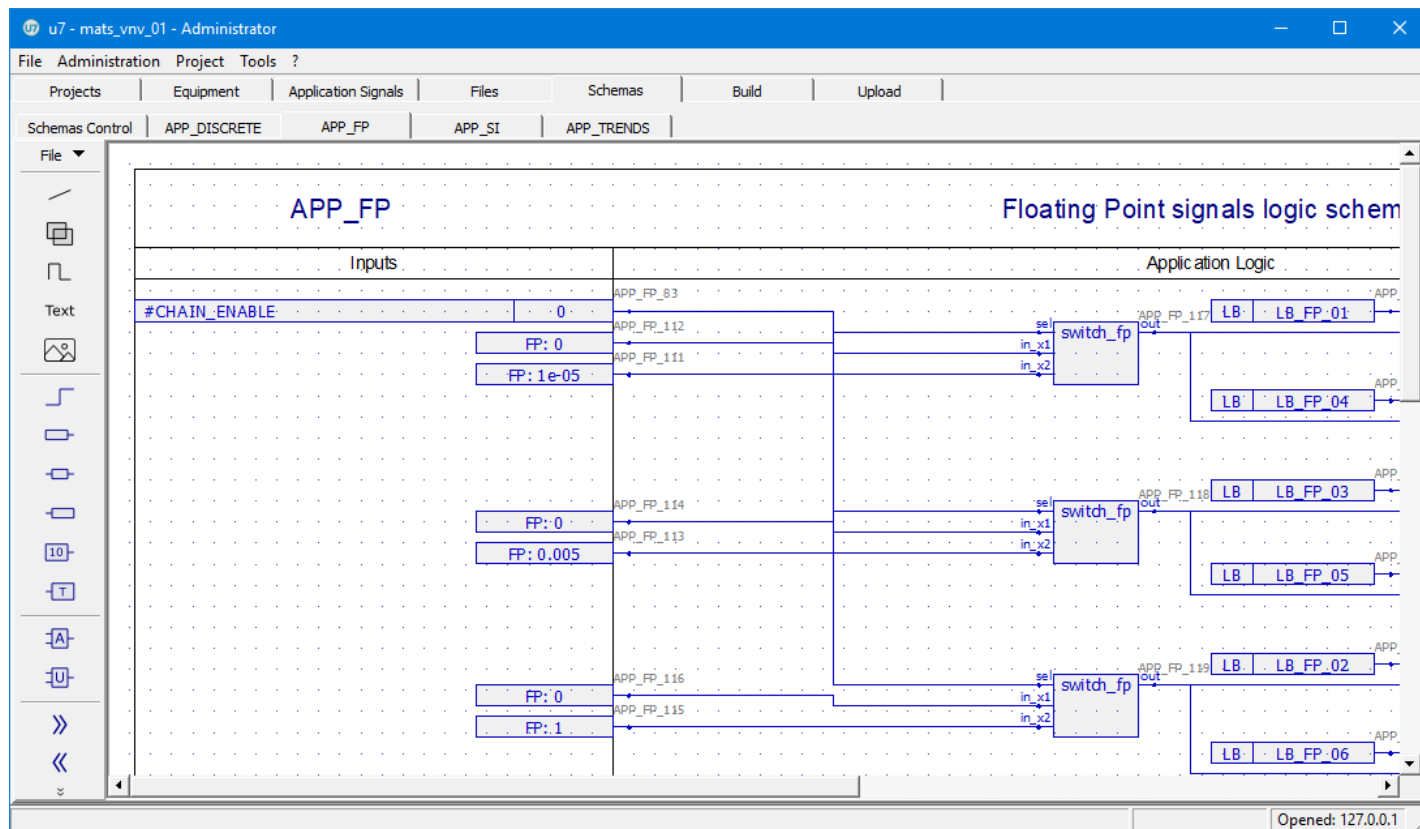
## 5 Electric parameters

ElectricHighLimit	10.0000
ElectricLowLimit	-10.0000
ElectricUnit	V
SensorType	Minus10_Plus10_V



# RPCT Integrated Development Environment (IDE)

## Design User Application Logic

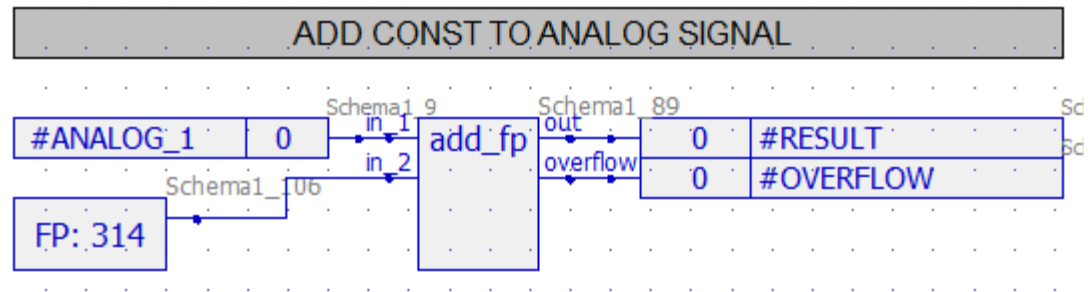


# RPCT Integrated Development Environment (IDE)

## User Application Logic elements

### Decoration:

- Lines, Rectangles, Text, Paths, Images.



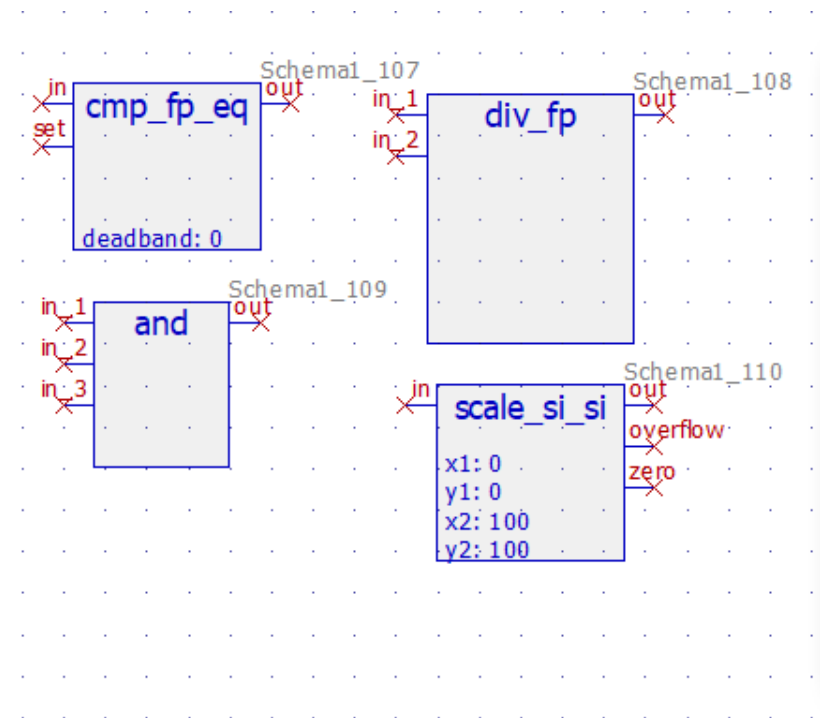
### Functional:

- Signals (input, output, in/out)
- Application Functional Blocks (AFB)
- User Functional Blocks (UFB)
- Links, Constants, Terminators
- Optical Transmitters / Receivers
- Bus Composer / Extractor, Loopback Source / Target

# RPCT Integrated Development Environment (IDE)

More than 100 AFB elements for UAL

- Comparison blocks
- Counters
- Type conversion blocks
- Dampers
- Time delay blocks
- FlipFlop blocks
- Discrete logic blocks
- Math function blocks
- Scaling blocks
- Bus operation blocks
- And many others





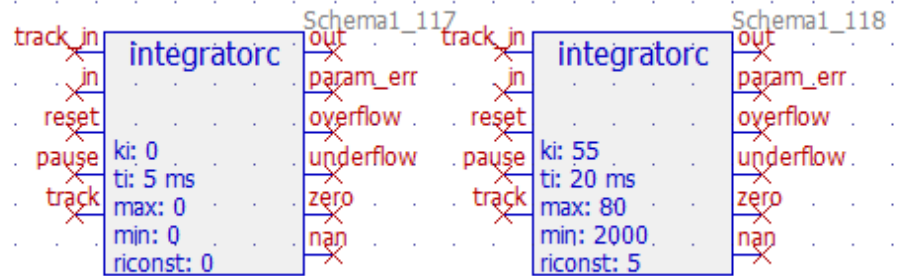
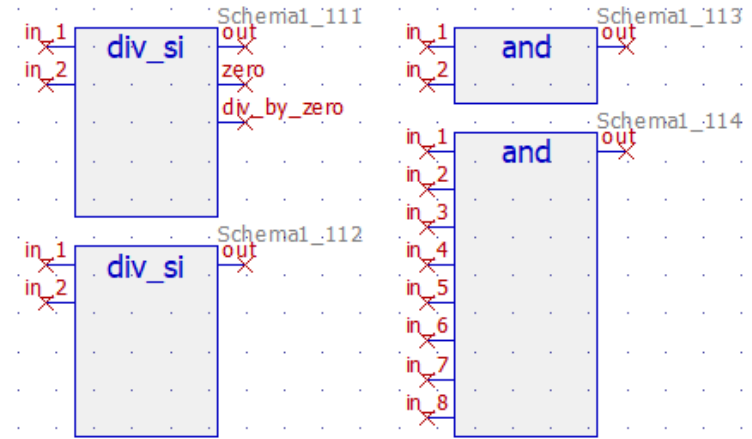
# RPCT Integrated Development Environment (IDE)

## User selectable pins in AFB

- Variable input count
- Optional outputs (errors, flags)

## User adjustable properties in AFB

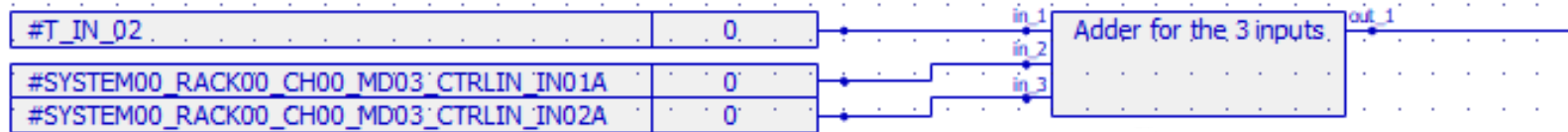
- RPCT controls correctness of entered values
- Properties can only be adjusted during project design



# RPCT Integrated Development Environment (IDE)

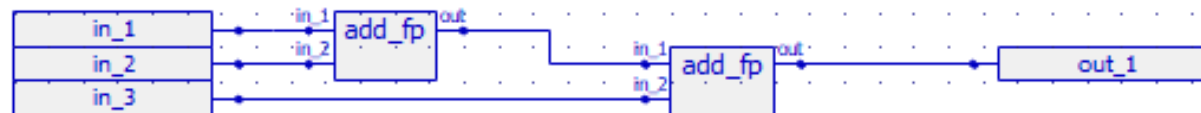
## User Functional Block (UFB Schema)

Designed from AFBs, reusing in UAL, implements complex logic



Adder for the 3 inputs

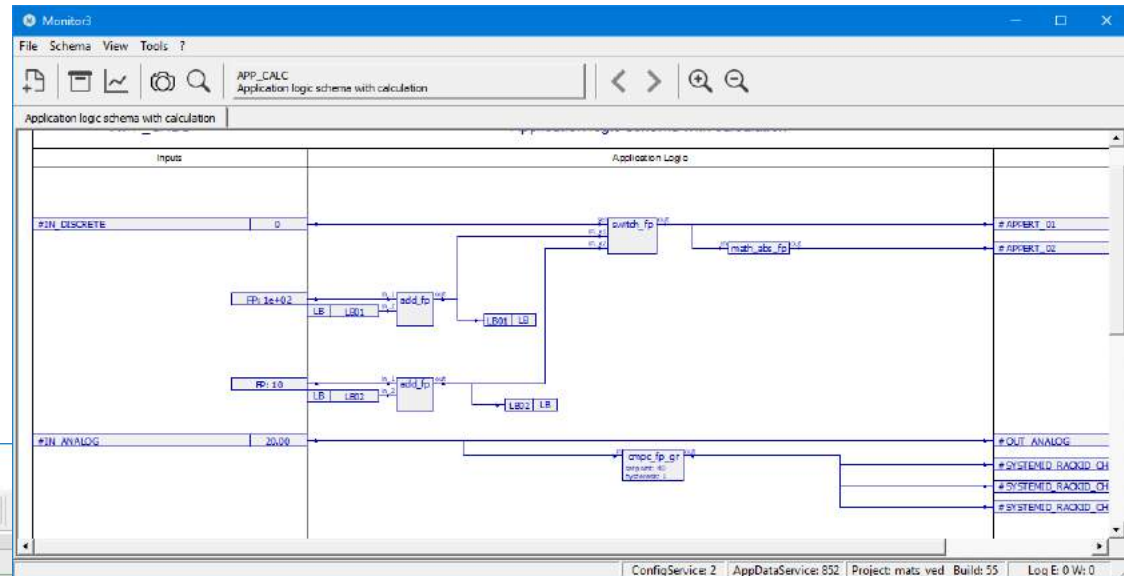
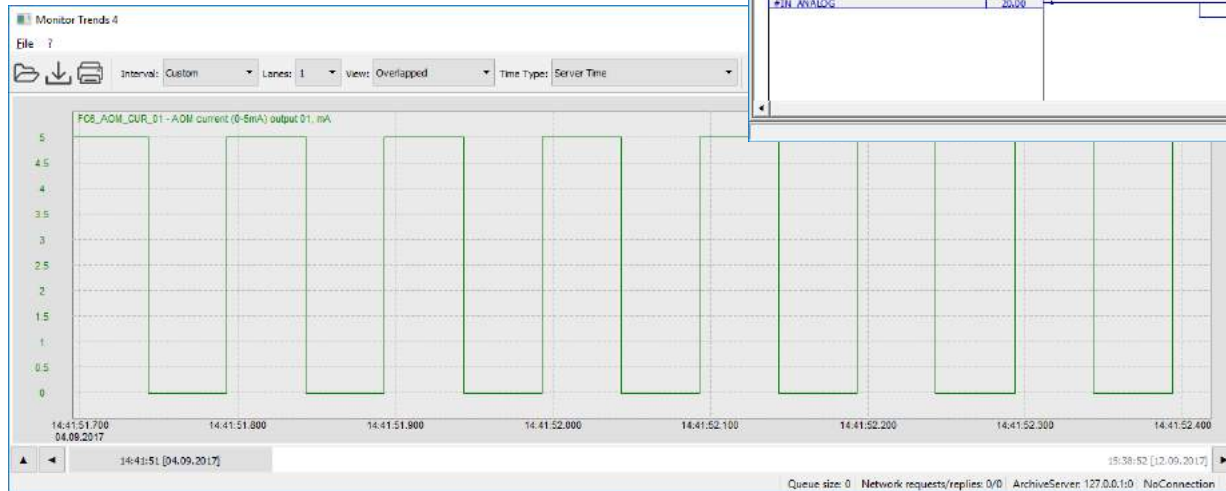
User Functional Block Logic



# MATS Components – Monitor

Visualizes:

- UAL Schemas
- Current states of signals
- Archive data (Trends, Tables)
- User Designed Schemas



# RPCT Integrated Development Environment (IDE)

## Monitor and Tuning Schema elements

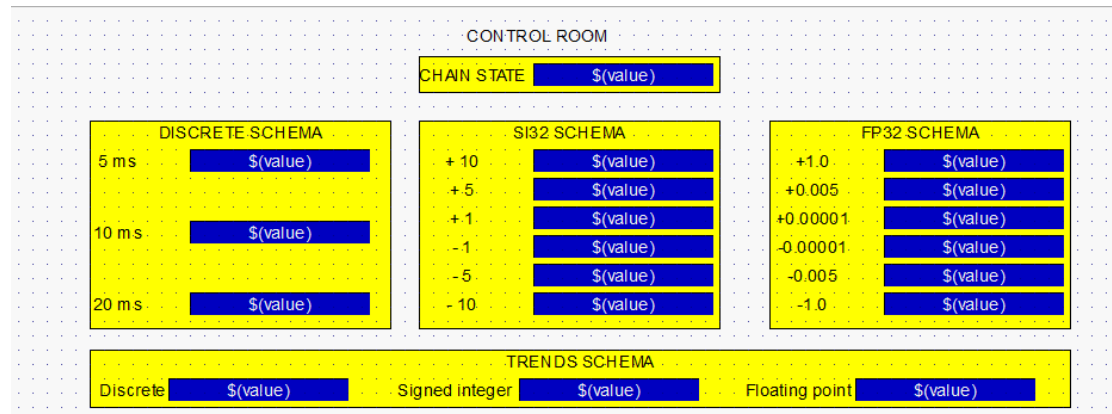
### Decoration:

- Lines, Rectangles, Text, Paths, Images.

### Functional:

- Value
- Image Value
- Push Button
- Line Edit

Functional behavior of some elements may be dictated by JavaScript



```
if(signalState == undefined)
{
    Text = "?";
    BackColor = "red";
    TextColor = "black";
}
else
{
    item.setPropertyValue("Text", Text);
    item.setPropertyValue("FillColor", BackColor);
    item.setPropertyValue("TextColor", TextColor);
}
```

# RPCT Integrated Development Environment (IDE)

## Project compilation

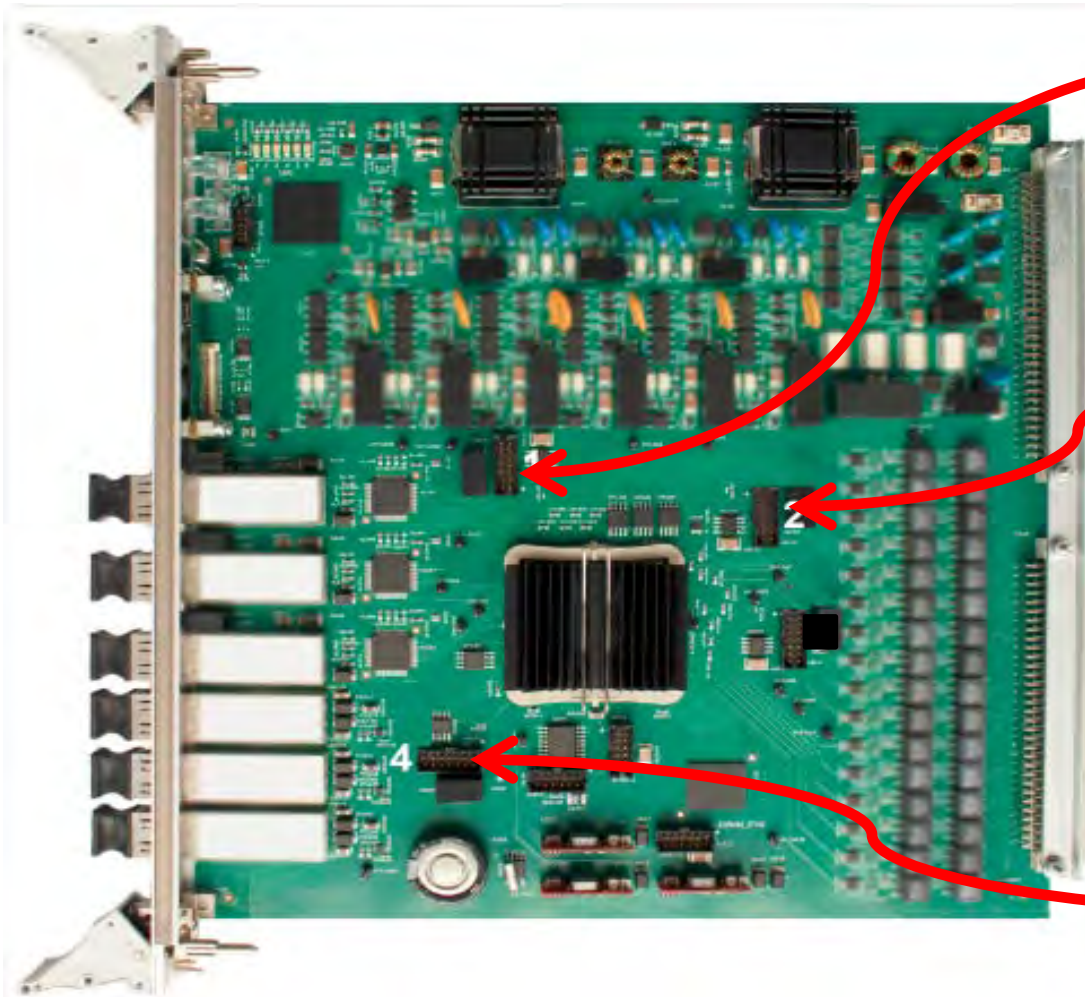
```
0000| 14:41:45:467 u7 v0.8.452 (master)
0001| 14:41:45:467 Started at: 05.08.2019 14:41:45
0002| 14:41:45:673 Opening project rpct_user_manual: ok
0003| 14:41:45:694 DEBUG building #2 was started. User - Administrator, host - DESKTOP-JLG64LM, changeset - 0.
0004| 14:41:45:695 WRN PDB2000: The workcopies of the checked out files will be compiled.
0005| 14:41:45:696 Build directory was created: C:/RPCT/rpct_user_manual-debug/build-000002
0006| 14:41:45:697 Build directory was created: C:/RPCT/rpct_user_manual-debug/build
0007|
0008| 14:41:45:700 Getting equipment
0009| 14:41:45:705 Getting equipment object, fileid: 1664, details: {"Type": ".hsm", "Uuid": "{1b4f950b-06c8-45e7-b6c9-1
0010| 14:41:45:970 Getting equipment object, fileid: 3076, details: {"Type": ".hsm", "Uuid": "{d339209e-99b7-4f39-93a7-7
0011| 14:41:46:006 Ok
0012|
0013| 14:41:46:007 Expanding devices StrIds
0014| 14:41:46:008 Ok
0015|
0016| 14:41:46:008 Checking for same Uuids and StrIds
0017| 14:41:46:010 ERR EQP6000: Property Place is less then 0 (Equipment object SYSTEMID_2_RACKID_CH01_MD-1).
0018|
0019| 14:41:46:011 DEBUG building #2 was finished. Errors - 1. Warnings - 1.
0020| 14:41:46:012 File was created: /build.log
0021| 14:41:46:021 Build time: 0 minute(s) 0 second(s)
```

# RPCT Integrated Development Environment (IDE)

## Compiler operations

- Equipment configuration check
- Application Signals parameters check
- User Application Logics schemas parsing
- UAL bitstream file generation for Logic Modules
- FSS configuration files generation
- MATS configuration files generation
- Timing and memory usage reports generation

# RPCT Integrated Development Environment (IDE)

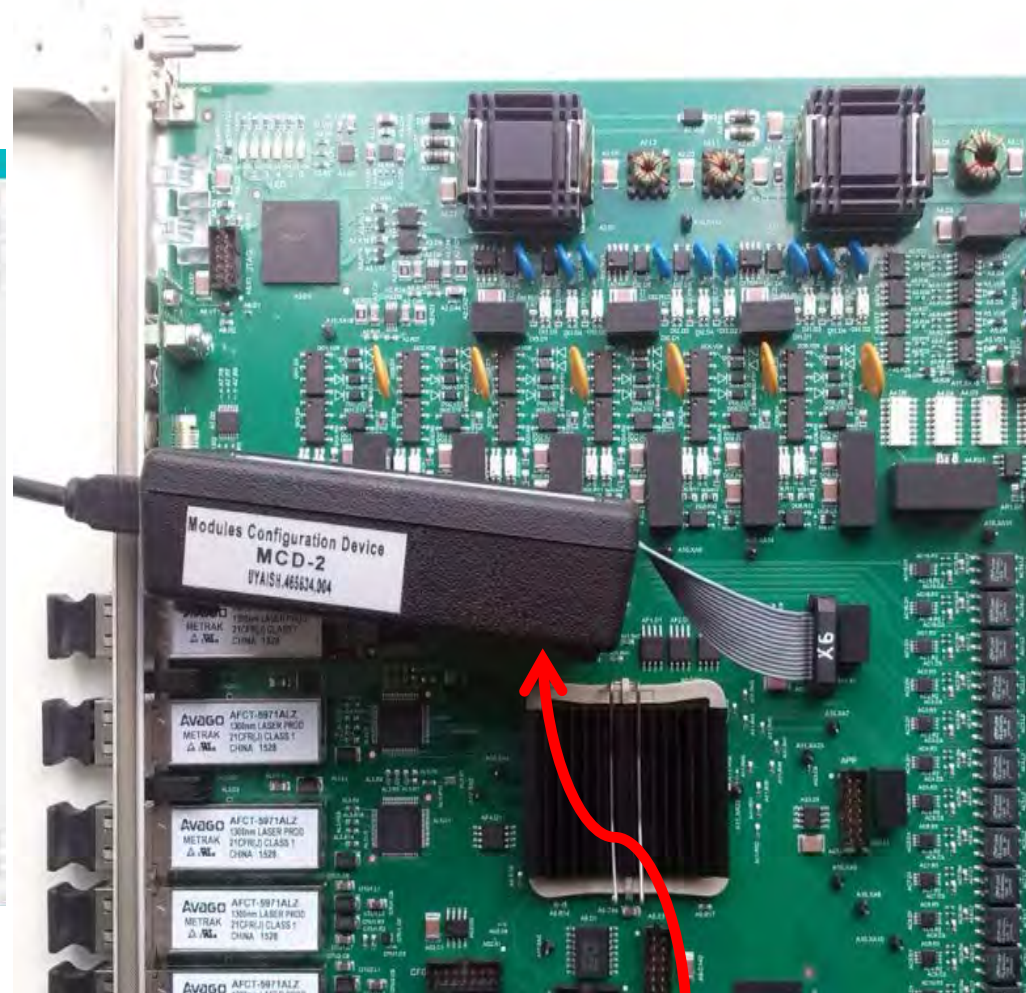
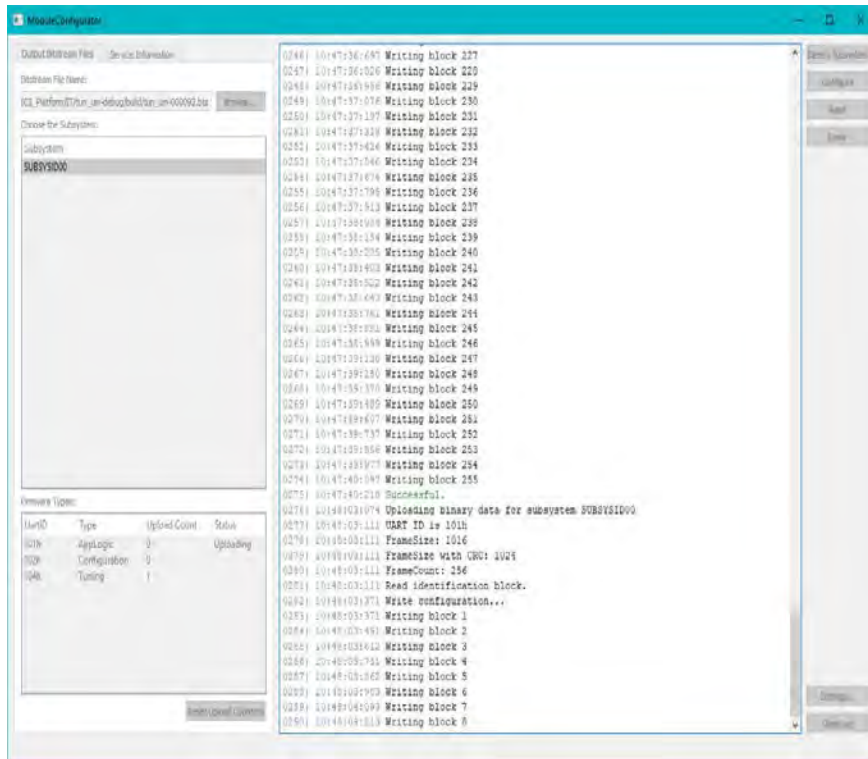


Set points  
configuration

User  
Application  
Logic

Hardware  
Configuration

# RPCT Integrated Development Environment (IDE)



Module Configuration Device



# Conclusions

- RPCT allows to design\verify I&C application without using HDL programming languages
- RPCT is completely home made tool with all the evidences required for licensing\qualification
- Later today (16:30 – 17:00) we will present an example of PID loop controller implementation using RPCT
- Later today (17:00 – 18:00) we will demonstrate operation of PID loop controller implemented in RadICS Platform

# Thank you for your attention!

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