# Role & development methods of FPGAs in Rolls-Royce safety Platforms

12th International Workshop on the Application of FPGAs in NPPs

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## Agenda

- Introduction
- Role of FPGA in Rolls-Royce I&C technologies
- Development, V&V, licensing
- Conclusion


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# 01 Introduction


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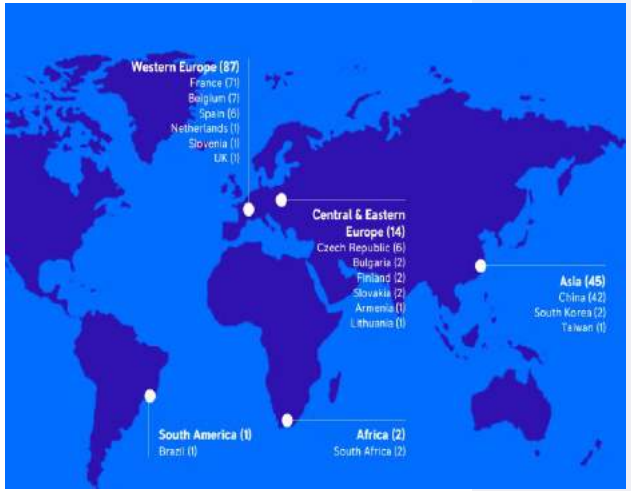
# Introduction




## Rolls-Royce Nuclear I&C

- 50+ years of experience in Nuclear I&C
- More than 140 reactors equipped with our I&C solutions
- Complete portfolio of I&C solutions

## Core safety I&C technologies based on:

- Microprocessor for Safety Digital platform
- Hardwired (relay-based) for non programmed safety platform

## At Rolls-Royce FPGAs are used for

- Simple electronic functions to complex application functions
- Existing boards, refurbishment
- Low complexity functions for safety equipment, high level of complexity for non-safety equipment (no embedded CPU)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02

# FPGAs in Rolls-Royce Technologies

- Rodline®
- Spinline®
- Hardline™


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## Rodline®

## Rodline is the latest generation of Rod Control System developed by Rolls-Royce

**The Rod Control System drives the Control Rod Drive Mechanism (CRDM)**

- Pilots the rods in individual steps by energizing the different electromagnets of the CRDM, in predetermined sequences
- One of the means to control the power of a nuclear reactor
- Non-safety

**Based on 40 years of experience**

- For retrofit and new build market
- References in more than 80 nuclear units


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## Modernization of 54 Rod Control Systems in France

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## New Build program in China

### 900MW nuclear fleet – 34 units

- VD3 (after 30 years of operation) – Partial modernization of the Rod Control System, including replacement of Cycler, control logic, processing logic and upgrade of power part
  - **32 units successfully modernized between 2008 and 2018**
  - **2 units to be modernized by 2020**

- VD4: modifications of the power cabinets, DC hold Cabinet, boards upgrades and evolutions of FPGA and monitoring HMI
  - **32 units to be installed between June 2019 and 2030.**

### 1300MW nuclear fleet – 20 units

- VD3 Full modernization of the Rod Control System by replacing existing systems with Rodline technology
  - **8 units successfully modernized between 2015 and 2018**
  - **12 units to be modernized until 2023**

### CPR 1000 fleet – 24 units

- Rod Control System for new build plants
  - **18 units successfully already delivered**
  - **4 00 Rodline Cabinets and 800 position detectors supplied**


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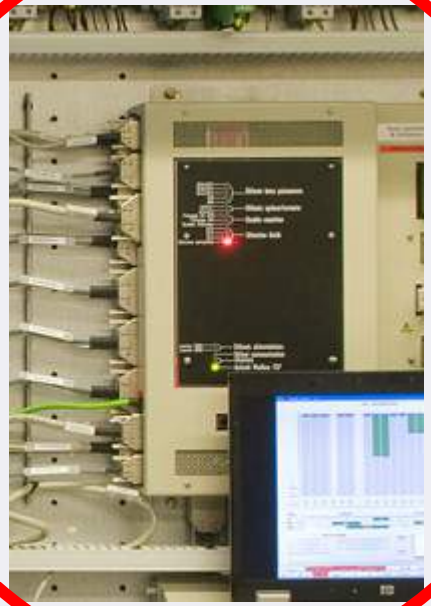


FPGA in Rolls-Royce I&C Technologies
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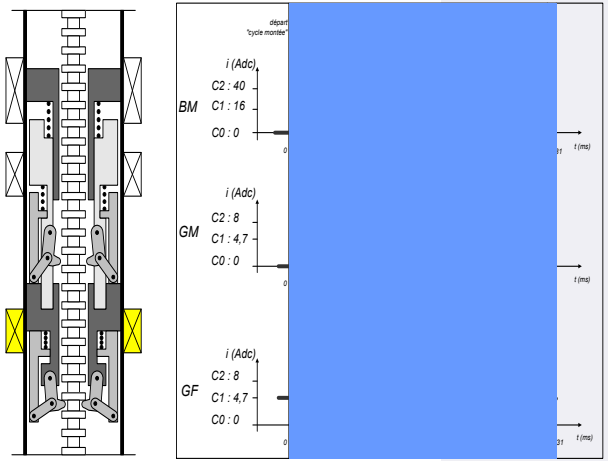
## FPGA for Cycler application

- 850 000 gates
- 157 I/O




**FPGA technology allows meeting stringent response time (1ms resolution) requirements difficult to fulfill with microprocessor**

**FPGA Flash technology allowing potential need for modification**

**FPGA implements 39 different functions including:**

- Generation of the control signals for the 3 coils that control the movement of the rods
- Selection and switching to the appropriate coil sets
- Check that the requested movements have actually been performed, in particular through the checking of the coil currents
- Ensure surveillance functions (consistency of the required sequences, power availability…)
- Safe states orders (double hold)
- Interface with the local HMI which can be used to manually control the rod positions
- Interface with the PLC-based control and diagnostic unit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## Spinline®

Spinline is Rolls-Royce latest generation of digital technology specifically designed for nuclear safety I&C applications

# Spinline platform allows building I&C safety systems to monitor and control nuclear reactors

- Meets licensing requirements for Cat. A / class 1E applications
- Can implement systems such as:
  - Reactor Protection Systems (RPS)
  - Neutron Instrumentation Systems (NIS)
  - Backup or post-accident systems (PAMS/SAMS)
  - Diesel I&C
- Adapted to New Builds and modernizations, for all types of nuclear plants
- Spinline is currently installed and operating in more than 90 plants in the world


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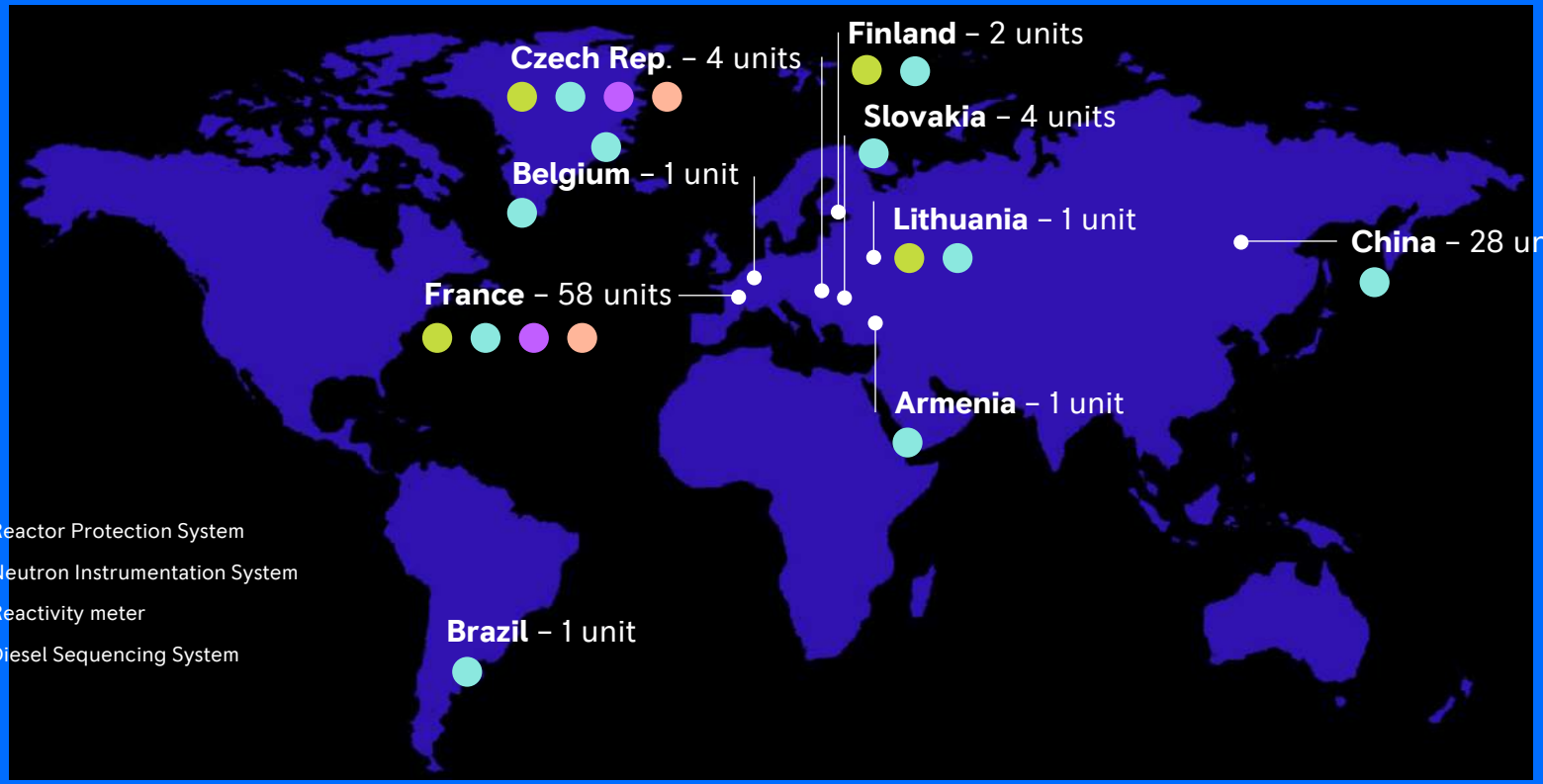
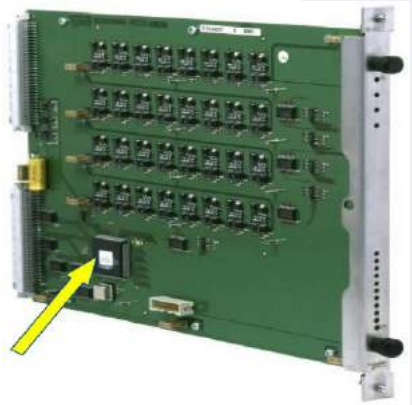



## References

More than 50 years and 1540 reactor years of experience worldwide, through multiple retrofit programs and new build projects

## Spinline®

## 32 Actuator Board design



## Previous actuator board: 1 microprocessor + logic circuits → board with FPGA:

- Electronic function implemented in Microchip (Microsemi /Actel) FPGA
- 30 000 gates
- Performs the following functions:
  - Bus interface
  - Processor interface (registers)
  - Surveillance of the outputs, using a short impulse test
  - Board self-tests
- All other components on the board are analog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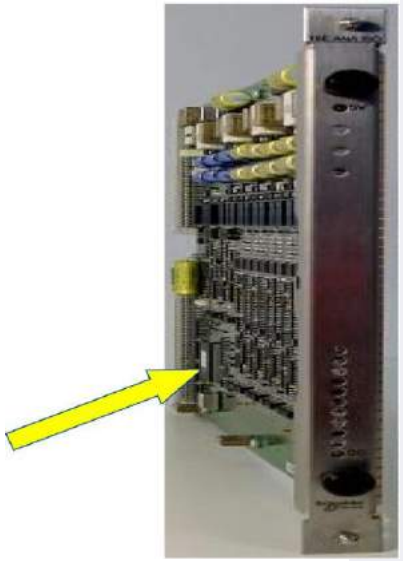
## Spinline®

## 16 Analog Input Board



## Previous analog board: 1 microprocessor + logic circuits; 6 analog channels per board → board with FPGA:

- The electronic function is implemented into a Microchip (Microsemi /Actel) FPGA
- 40 000 gates
- Performs the following functions:
  - Interface with the bus
  - Control of acquisition (16 inputs in 1 ms)
  - For each input, processing of the input value for gain & offset adjustment, performed by an Arithmetical & Logic Unit
- Board self-tests
- All other components on the board are analog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## Spinline®

## Neutron Instrumentation System

### Conditioning board (COND CGD): Analog Amplifier, High voltage generator and logic circuits → board with FPGA:

- Electronic function implemented in Microchip FPGA
- Safety Classification: 1E (RCC-E 2005), Cat. A
- 27,696 DFF (Flip-Flop)
- Performs the following functions:
  - Impulse calibration
  - MSV (Mean Root Square) calculation
  - Current measurement
  - High Voltage Controller
  - Maintenance/LDU Communication
  - Impulse test
  - Board self-tests
  - All other board components are analog

### + I/O board (SIO): I/O → board with FPGA


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## Hardline™

**Cat. A / class 1E for**

- **Diverse Protection Systems (DPS)**
- **Actuator Priority Logic Systems (PLS)**
- **Backup or post-accident systems (PAMS/SAMS)**
- **Main Reactor Protection System (Retrofit, Research reactor & SMR)**

# HardlineTM: Rolls-Royce latest generation of hardwired technology designed for nuclear safety I&C

- Based on non-programmed discrete components
- Advanced Integrated monitoring & Diagnosis features
- Reduced footprint & internal cabling
- Standard cabinets allowing delayed differentiation
- Quick setup from design to installation
- Optimized engineering system tools


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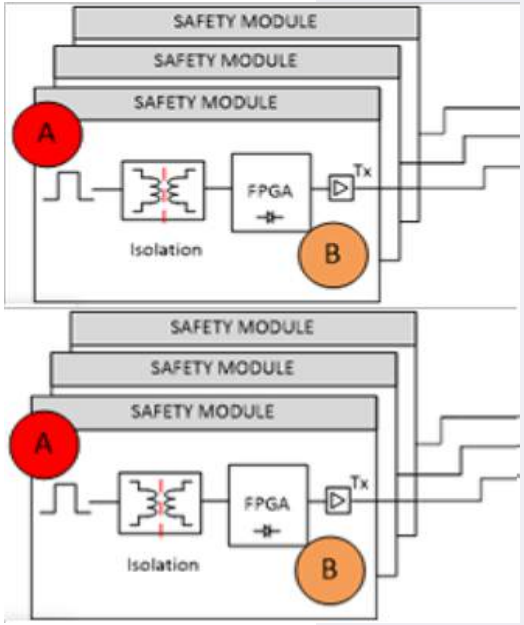
## Hardline™

## Existing




## FPGAs in Hardline are used for several functions:

- **Supervision** (1 FPGA): Data acquisition from binary or analog signals, transmission to serial link.
- **Gateway** (3 FPGAs): Aggregation of the data from all the communication boards and equipment status (binary inputs), and transmission to Spinline or PLC (protocol conversion)
- They are **NOT used for process functions**

## To summarize, Hardline FPGAs:

- Mainly aggregate data (inputs + local defaults status)
- Transmit them (possibly with protocol conversion serial ←→ Modbus/Tcp/Nervia)
- Check data validity on the fly
- Can be parameterize to adapt to configuration changes (board numbers, data size/format…)
- These supervision functions are electrically isolated from process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# 03

# Standards, regulations & V&V approach


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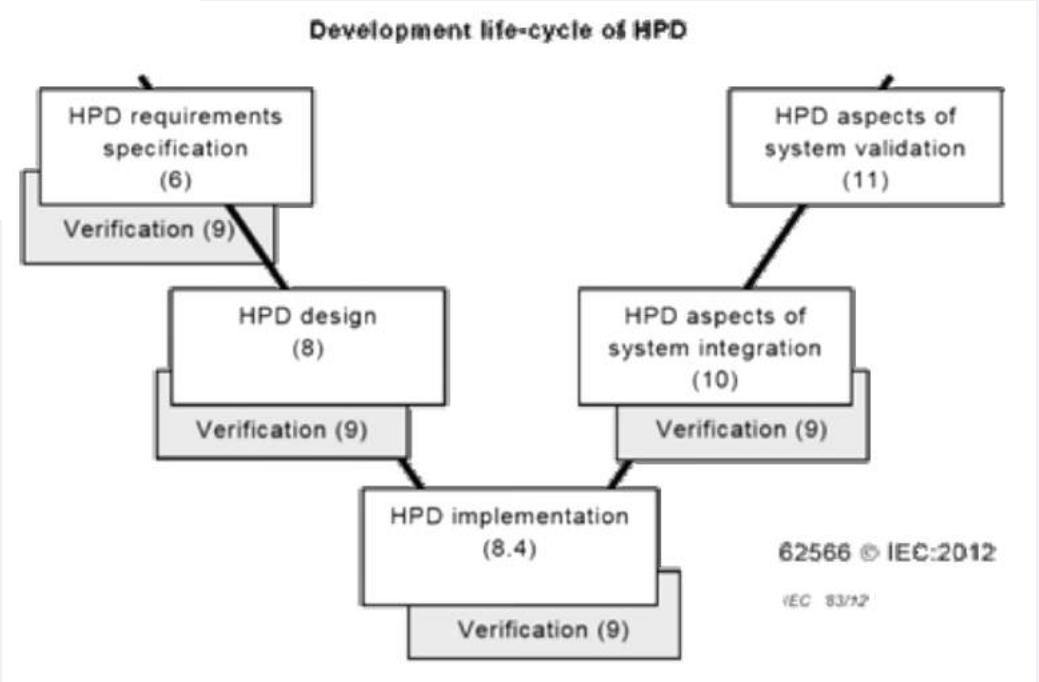
# FPGA Design Flow of electronic boards for class 1 equipment

- Successfully used for all electronic functions design
- Compliant with IEC62566
- Entirely and exclusively applied in the Hardware electronic department
- Pre-Developed Blocks NOT used
- **Applied to more than 25 class1 boards**





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# Spinline licensing

UNITED STATES, US NRC:

Spinline: safety evaluation of the Spinline generic platform

FRANCE, ASN/IRSN:

EDF - VD3 1300MW: Plant specific project

20 NPP refurbishment currently in deployment phase

FINLAND, STUK:

FORTUM - ELSA project: Plant specific project

Successful refurbishment of I&C systems at the Loviisa NPP (2018)


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# 04 Conclusion


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## FPGA use evaluation

(without embedded CPU)

## FPGA benefits for electronic functions

- Flexibility and ease for implementing hardware functions
- Reduction of discrete components, higher board reliability
- Replacement of sensible and/or obsolete components

## Specific skills needed

- Design and test activities require dedicated skills with electronic hardware background rather than System or software background
- HDL coding differs significantly from software coding
- Architecture of the FPGA and targeted design must be well understood and drive the design beyond the functions to implement

## Need for technical attention

- No easy for floating point calculation, developing an FPU was needed
- No easy implementation of complex functions
- Partitioning, separation, local specific redundancy, parallel propagation
- Design and testing tool behavior (tools validation)
- Parameter handling (conditions & processes for changes)


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## Conclusion

- FPGA bring additional possibilities to Software or hardwired based technologies
- Development, V&V must follow rigorous process
- Licensing difficulty similar to software for complex applications
- Specific skills must be mastered


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