



HF Controls

# HFC-FPGA System Equipment Qualification and Lessons Learned



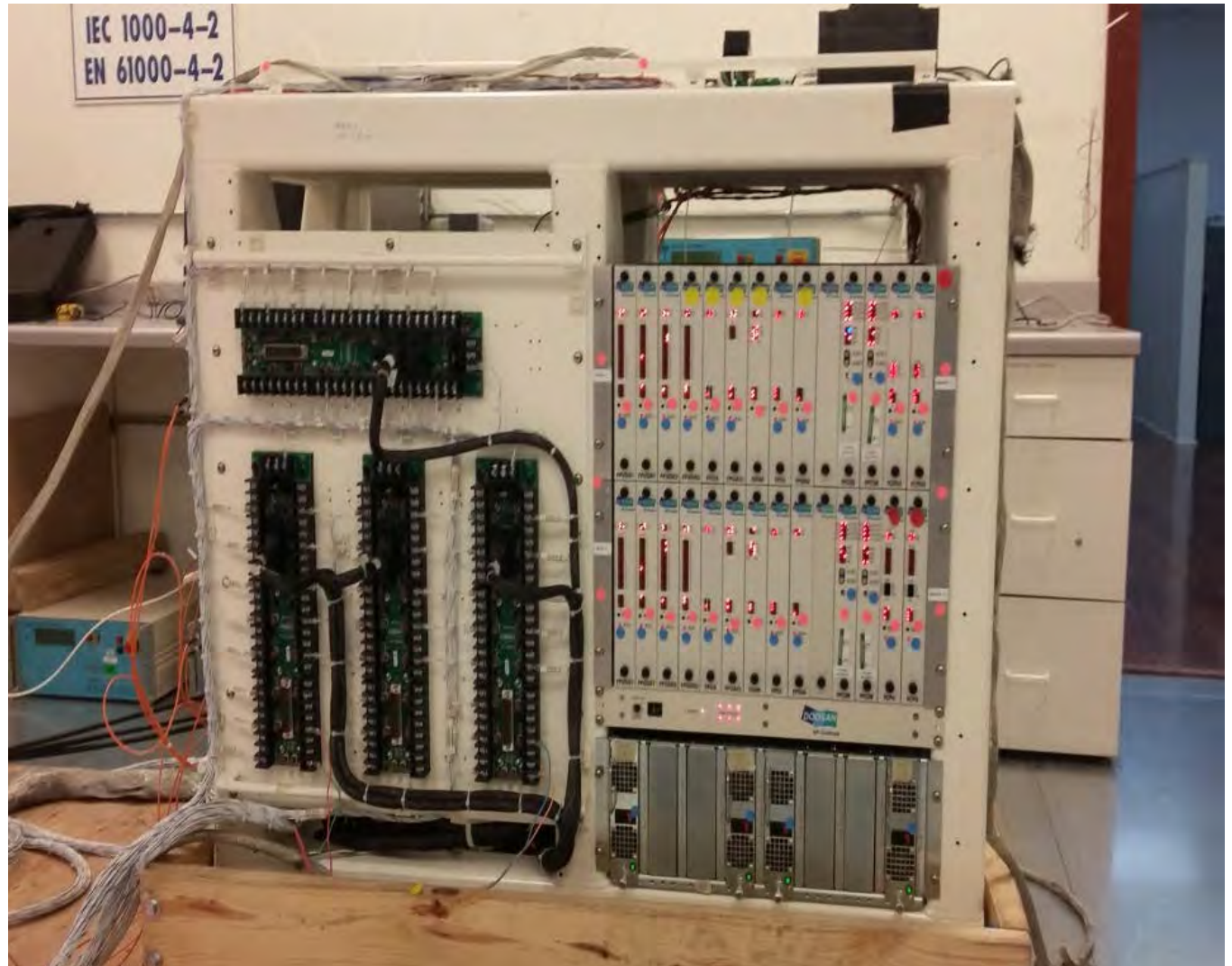
October 10<sup>th</sup>, 2018

# Table of Contents

- Test Specimen
  - Configuration
  - Modules
  - Redundancy
- Test Sequence
  - Burn-in
  - Baseline testing
  - Heat and Humidity
  - EMI/RFI
  - Seismic
  - Post-stress Operability and Prudence
- Lessons Learned
  - Burn-In
  - Baseline testing
  - Heat and Humidity
  - EMI/RFI
  - Seismic
  - Post-stress Operability and Prudence

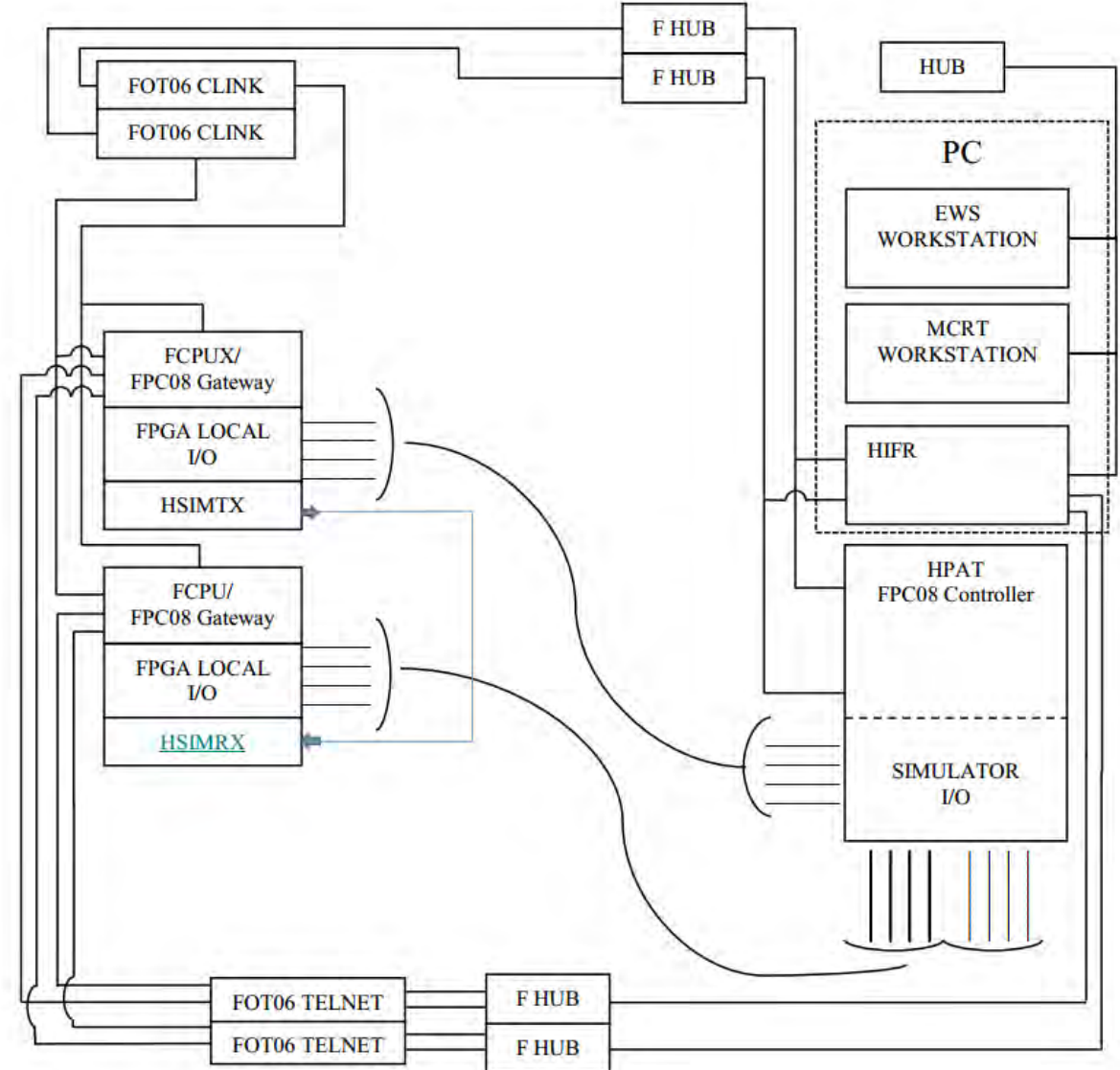
# Test Specimen: Configuration

- Two remotes in a seismic rack
  - Remote 1: FCPU
  - Remote 2: FCPUX
  - All associated Termination Boards
  - All associated CON cards on backplane
- Incoming 120 VAC power
  - To 24 VDC redundant Power Supplies
  - Line Filters and Surge Suppressors
- Outgoing signal lines to HPAT
  - HFC Programmable Automated Tester
  - Unshielded during normal operation
  - Fiber optic communication to HPAT
- All FPGA used are Microsemi
  - ProASIC3
  - IGLOO
  - IGLOO2



# Test Specimen: Configuration

- FPC08 Gateways
  - Communicate between FPGA Controllers and C-Link
  - Modified version of previous HFC-FPC08 controller
- HSIMTX/HSIMRX
  - Fiber optic F-Link communication modules
  - Allows for communication of I/O points between racks
- HPAT
  - Custom application to support testing
  - Field wiring to Test Specimen I/O points
  - Analog and Digital Inputs and Outputs
  - Communicates with Engineering Workstation PC via Ethernet



## Test Specimen: Modules

Designation	Function
HFC-FCPU	Master Controller with 4 DI/4 DO
HFC-FCPUX	Master Controller
HFC-FPUA	16-Point Analog Input
HFC-FPUM	8-Point 3-Wire RTD Input Card, 100-ohm Platinum
HFC-FPUM2	8-Point 3-Wire RTD Input Card, 100-ohm Platinum (High accuracy)
HFC-FPUL	8-Point E-Type Thermocouple Input Card 0-500 °C
HFC-FPUAO	8-Point Analog Output Card (4-20 mA)
HFC-FPUD01	16-Point Form C Relay Outputs + 16-Point Discrete Inputs
HFC-FPUD02	32-Point Discrete Input Card (24, 48 VDC input)
HFC-FPC08	Communication Gateway Controller
HFC-HSIM	High Speed Interface Module

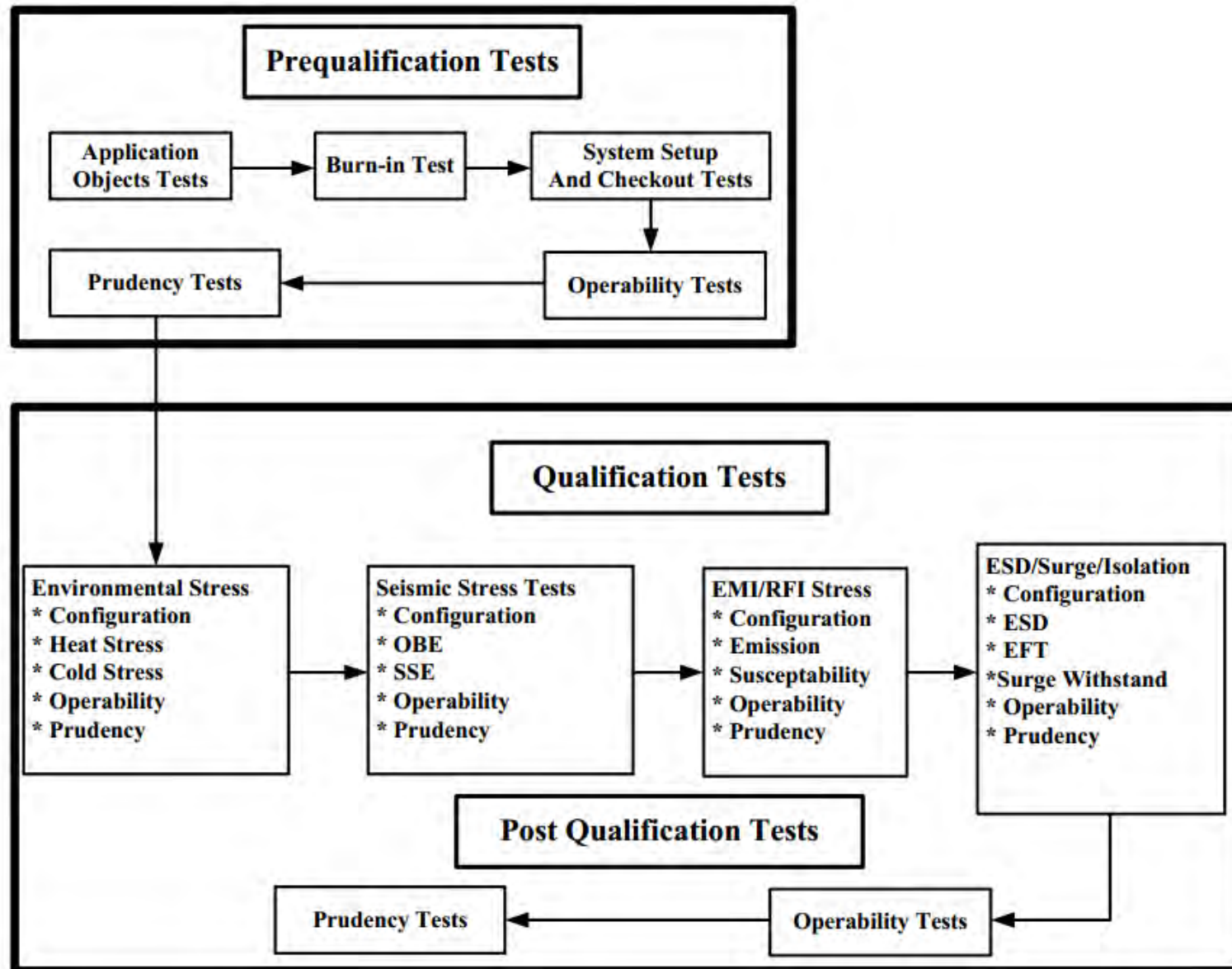
# Test Specimen: Redundancy

- Remote level
  - Two remotes with nearly identical test applications
  - In the event of remote crash, module data available from other remote
- Master Controller
  - Each remote has two redundant FCPU/FCPUX
  - In the event of primary controller failure, failover occurs and the remote continues to function
- Communication Gateway
  - Each remote has two redundant FPC08 Gateways
  - Allows for continued communication with EWS PC in the event of a single failure
- Onboard FPGA
  - HFC-FPGA modules have a Control and Diagnostic FPGA on-board
  - Diagnostic running in parallel to detect failures
  - No on-board failover
- 24 VDC Power Supplies

# Test Sequence: Overview

- Performed as part of Test Phase
  - All components of EQ test system must be version controlled
  - All implementation phase tasks must be completed on Test Specimen Hardware and FPGA loads
  - Traceability to previous phases to ensure correct testing is done at the correct levels
- Software tools
  - Historical Archiving System (HAS) for point transitions and analog data
  - Sequence of Events (SOE) Logger for ms-resolution DI/DO transitions
  - HFC OneStep for translation of application from PromisE to FPGA load
  - All SW tools are released and version controlled
- FPGA loads
  - Timing analysis completed
  - All other tests that may result in code changes completed

# Test Sequence: Overview





# Test Sequence: Burn-in Test

- Performed per EPRI TR 107330
- In-house, non-destructive test
  - No special equipment required
  - Ambient atmospheric conditions
- All PCBs must be powered on and in a normal operating state for 352 hours
  - In communication with controllers
  - Running TSAP
  - Run time is cumulative and the test may be started or stopped without failure
  - The failure of a single board does not constitute the failure of an entire rack or assembly
- PCBs that pass the Burn-in Test may be used for production or EQ testing
  - Used to detect early-life failures in PCBs
  - Failing boards will undergo Root Cause Failure Analysis

# Test Details: Burn-in Test (Continued)



Powered on  
TSAP running  
All cards present

DMT LED on solid

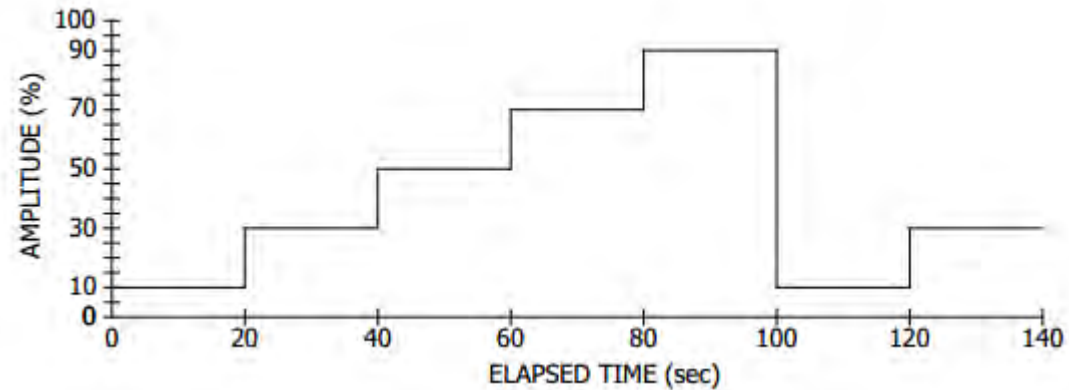
A/B not hunting

TX/RX flashing to indicate communication



# Baseline Test: Operability

- Performance tests to determine Test Specimen performance during and following EQ tests
  - Baseline results determined during pre-qualification tests
  - Results from EQ testing compared to baseline to evaluate impact of EQ test on Test Specimen
- Accuracy for Discrete and Analog I/O
  - Manual Accuracy measurements on each module
  - Automated accuracy testing and measurement during Qualification



# Baseline Test: Operability

- Response time for Discrete and Analog I/O
  - Response time measured using an oscilloscope for analog and digital channels
  - Automated response time testing performed during qualification testing

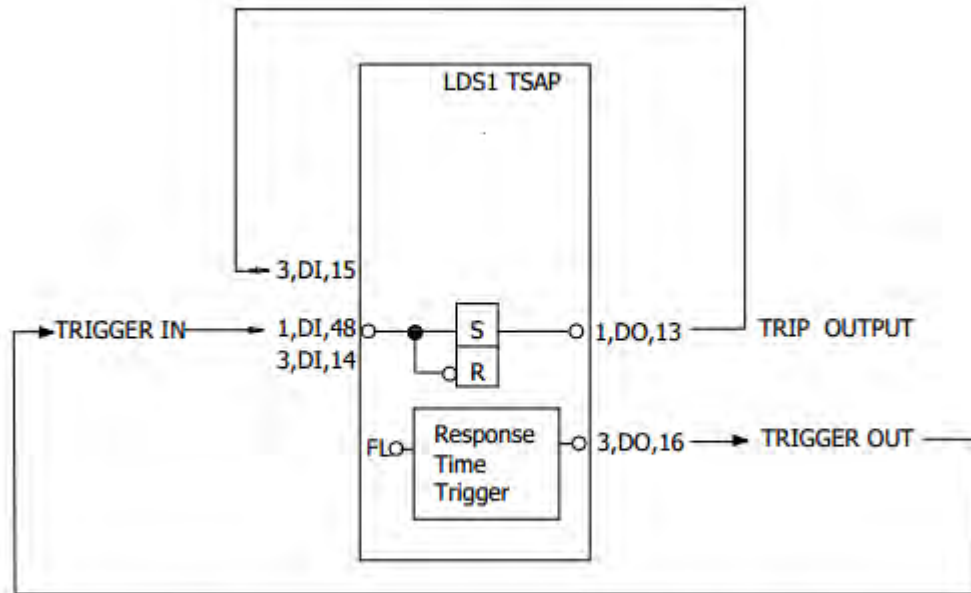


Figure 2. LDS1 TSAP Algorithm for Digital Response Test

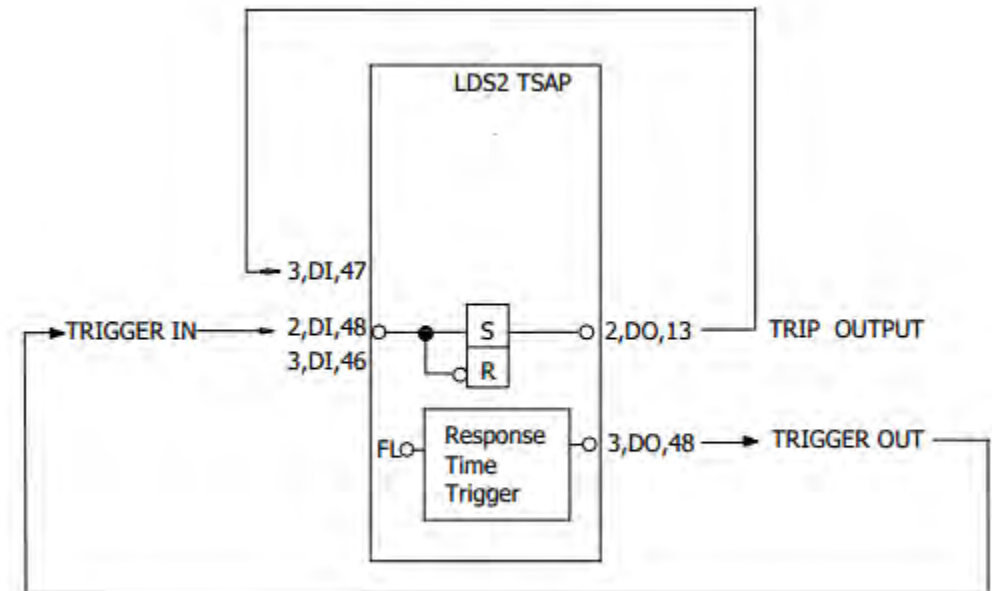


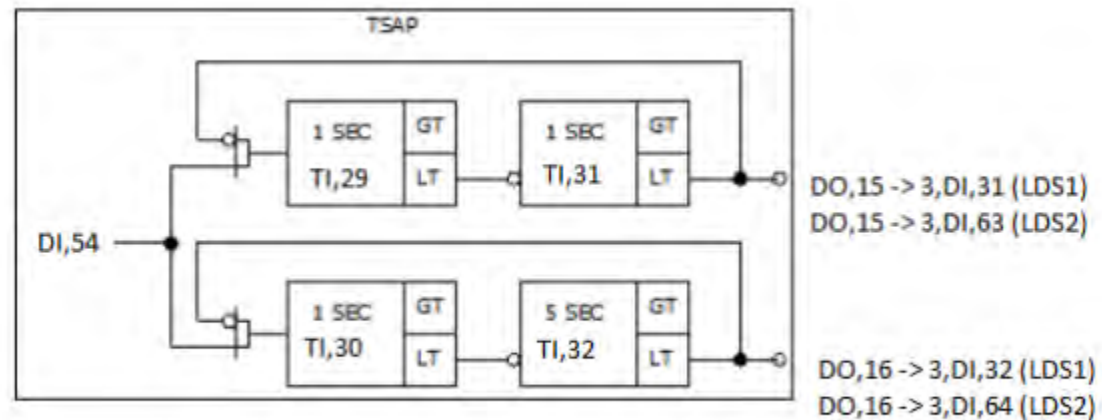
Figure 3. LDS2 TSAP Algorithm for Digital Response Test

# Baseline Test: Operability

- Discrete Input Operability
  - State transitions measured at intended voltage
  - State transition low voltage measured
  - State transition high voltage measured
  - Not performed during qualification testing due to need for Test Specimen access
- Discrete Output Operability
  - State transition measured at intended current draw
  - State transition measured at lowest designed current
  - State transition measured at highest designed current
  - Not performed during qualification testing due to need for Test Specimen access
- Communication Operability
  - All communication links monitored for complete and correct data transfer
  - Comparison of sent and received packets
  - Periodic data transmission
  - Performed during qualification testing

# Baseline Test: Operability

- Coprocessor Operability
  - Not performed in HFC systems as it is not applicable
  - Measurement of loop times for coprocessors
  - Operability functions of coprocessors tested
- Timer Tests
  - Timers are set to toggle I/O points and analog values in a periodic pattern
  - State transitions for these I/O points are monitored and the period of transition is analyzed
  - Conducted during qualification testing



**Figure 6.** TSAP Timer Test Algorithm

# Baseline Test: Operability

- Failure to Complete Scan detection
  - Self-diagnostics or other internal system monitoring uses periodic scans of data by the PLC
  - Induces a communication fault or break to cause a scan failure
  - Measure the response time of the system between inducing and detecting failure
  - Not conducted during qualification testing due to required access to the Test Specimen
- Failover Operability
  - Redundant components of the system are removed or powered off to induce failover
  - Controllers, communication gateways, power supplies
  - Other automated tests such as accuracy and timer tests are run to evaluate Test Specimen response
  - Not conducted during qualification testing due to required access to the Test Specimen
- Loss of Power
  - Incoming power to the Test Specimen removed for at least 30 seconds
  - Power restored to Test Specimen
  - Other automated tests such as accuracy and timer tests are run to evaluate Test Specimen response
  - Not conducted during qualification testing due to required access to the Test Specimen

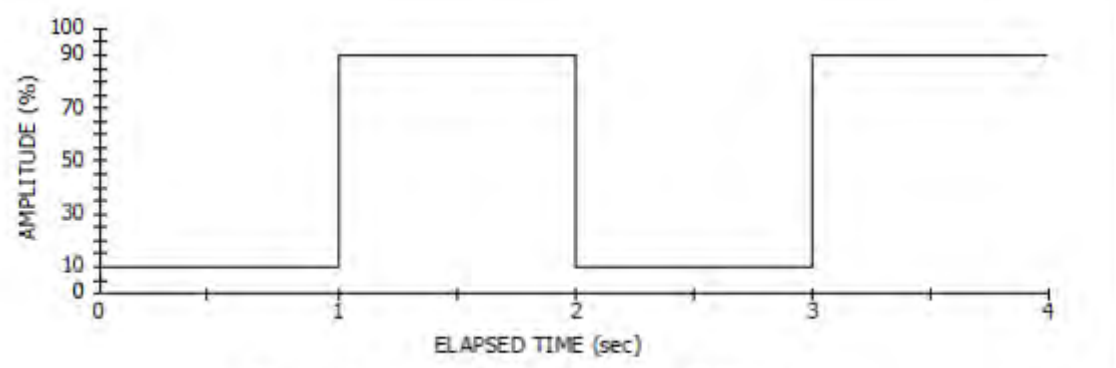
## Baseline Test: Operability

- Power Interruption
  - 40 ms loss of power induced on incoming unit power
  - UPS can be used to mitigate the impact, if included in general qualification of the PLC
  - Other automated tests such as accuracy and timer tests are run to evaluate Test Specimen response
  - Not conducted during qualification testing due to required access to the Test Specimen
- Operability testing performed before, during and after qualification tests
  - All tests done before and after qualification
  - Automated Accuracy, Response Time, and Timer tests performed during qualification testing
  - Acceptance criteria defined in EPRI TR 107330



# Baseline Test: Prudence

- Performance test to determine the response of the test specimen to the EQ tests
  - Baseline test performed during pre-qualification phase
  - Results during and after EQ testing compared to baseline to identify performance changes
- Burst of Events
  - DI/DO channels toggling at a 1 Hz frequency
  - AI/AO channels toggling between 10% and 90% at a 1 Hz frequency
  - Serial I/O scanning is an automatic function of the controller and requires no test configuration.
  - Conducted during qualification testing



*Figure 1 – Algorithm for Analog BOE Test*

# Baseline Test: Prudence

- Serial Port Failure
  - Redundant serial ports internal to the Test Specimen and performing external communication are disconnected
  - Automated tests are run during these port failures to assess Test Specimen response
  - Conducted using a breakout cable
  - Not conducted during qualification testing due to required access to the Test Specimen
- Noise Test
  - Superimposes a 100 kHz white noise signal at 2.5 vrms
  - Imposed on the transmit and receive signal lines of each serial port
  - Not conducted during qualification testing due to required access to the Test Specimen
- Fault Simulation Test
  - Simulates failure of primary controller in a remote to trigger failover to secondary controller.
  - Not conducted during qualification testing due to required access to the Test Specimen

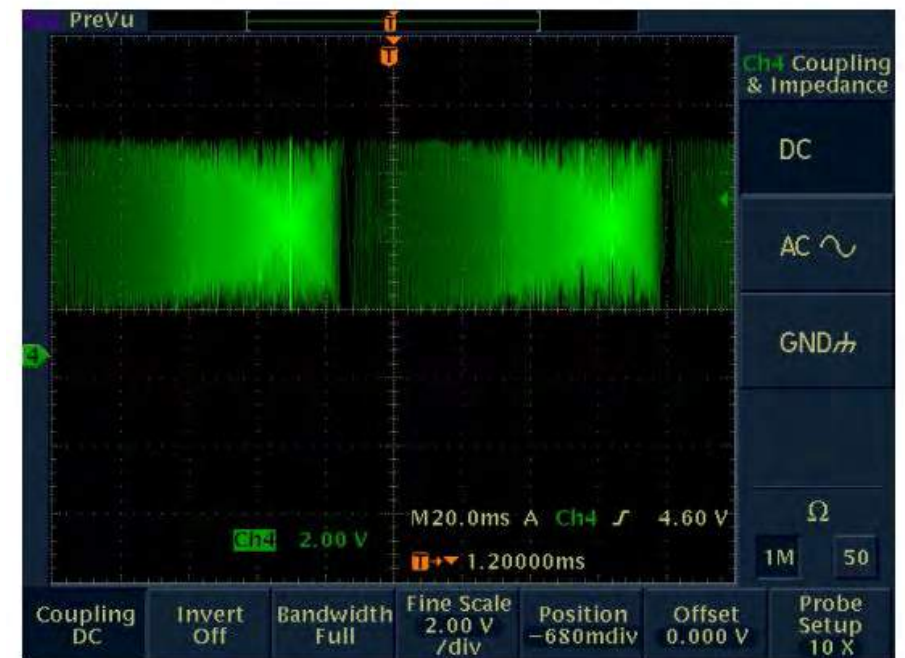


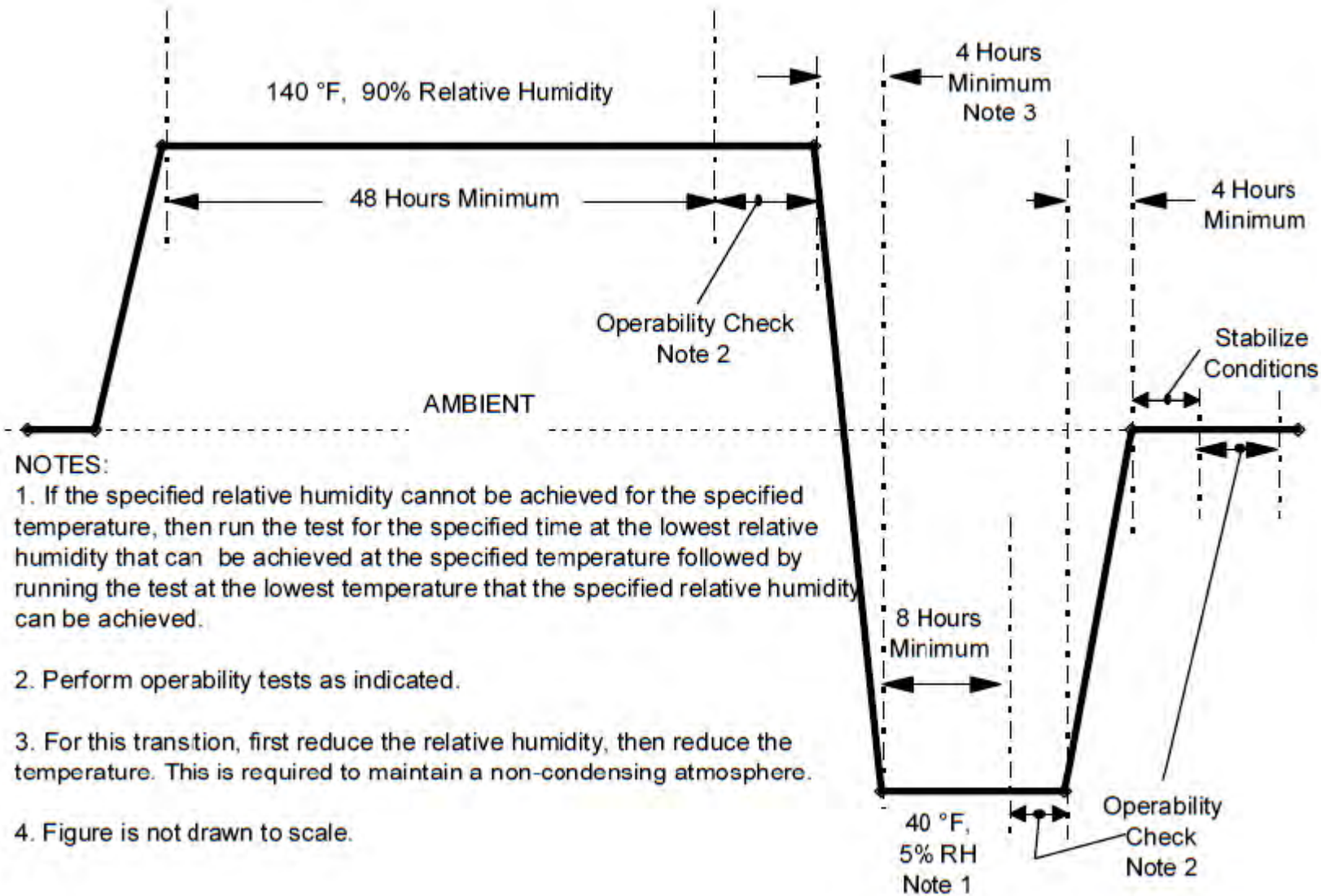
Figure 2 – Noise Signal Waveform

# Test Details: Environmental Stress Test

- Per EPRI TR 107330 4.3.6
- Laboratory test, potentially destructive test
  - Temperature and humidity controlled chamber
  - Calibrated thermocouples
- Test Specimen is running and in normal operating configuration
  - Located in climate-controlled test chamber
  - Connected via communication cable (Cat5) to external monitoring PC
- Operability and prudence checks run at specified times during the test
  - End of elevated temperature, end of low temperature, and end of test
- Test duration is specified by minimum durations
  - Allows for flexibility to accommodate lab personnel
  - Long transition times prevent condensation



# Test Details: Environmental Stress Test (Continued)



**NOTES:**

1. If the specified relative humidity cannot be achieved for the specified temperature, then run the test for the specified time at the lowest relative humidity that can be achieved at the specified temperature followed by running the test at the lowest temperature that the specified relative humidity can be achieved.

2. Perform operability tests as indicated.

3. For this transition, first reduce the relative humidity, then reduce the temperature. This is required to maintain a non-condensing atmosphere.

4. Figure is not drawn to scale.



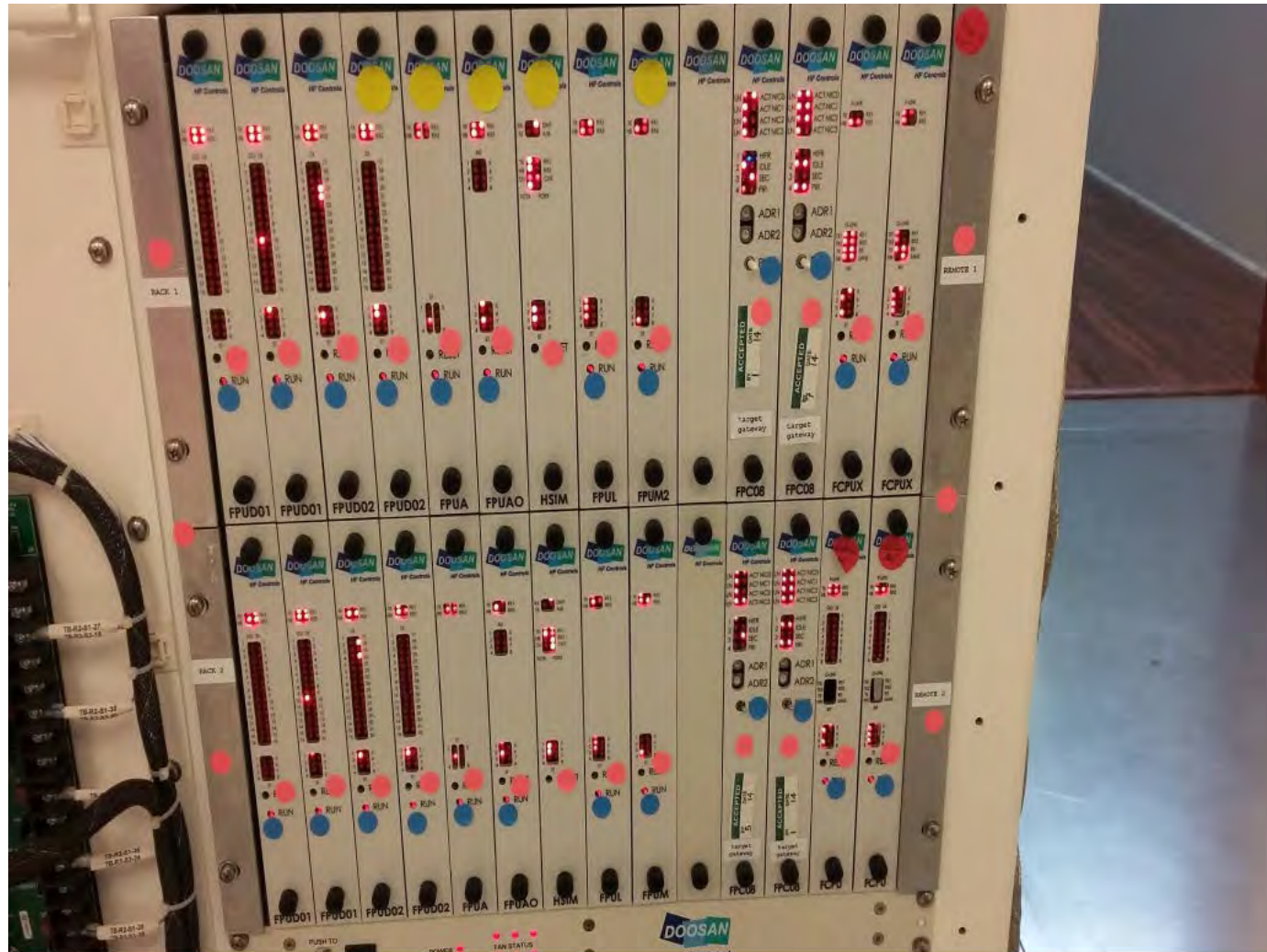
## Test Details: Environmental Stress Test (Continued)

- Automated tests
  - Timer Test
  - Automated Accuracy Test
  - Automated Response Time test
  - Burst of Events Test
- Operability checks at specified points
  - Loss of Power Test
  - Failover Test
  - Automated Tests
- Margins
  - EPRI TR-107330 requires margins on test envelope to ensure test meets or exceeds envelope
  - $\pm 5^{\circ}$  F and 5% Relative Humidity

# Test Details: Electrostatic Discharge Test

- Per IEC 61000-4-2
- Laboratory test, potentially destructive testing
  - ESD pulse generator
  - Ground plane
- Test Specimen is running in normal configuration
  - Test points are all areas that may be accessed by operators
  - Areas inside cabinets are tested despite normal operation being ‘doors closed’
  - Automated Operability Tests and Burst of Events Test is running while pulses are applied
- Pulses are applied for contact and air discharges
  - Contact discharges are 8 kV, and applied to conductive surfaces (Card bezels, handles, frames, etc)
  - Air discharges are 15 kV, and applied to nonconductive surfaces (Switches, flat screen monitors, cords, ETC)
  - All test points are exposed to 10 discharges at both polarities
- Acceptable responses are either normal performance or temporary degradation
  - Normal performance means there was no degradation or deviation caused by the pulses
  - Temporary degradation means that any deviation from normal performance was corrected without operator intervention

# Test Details: Electrostatic Discharge Test (Continued)



HFC-FPGA Rack Front Test Points

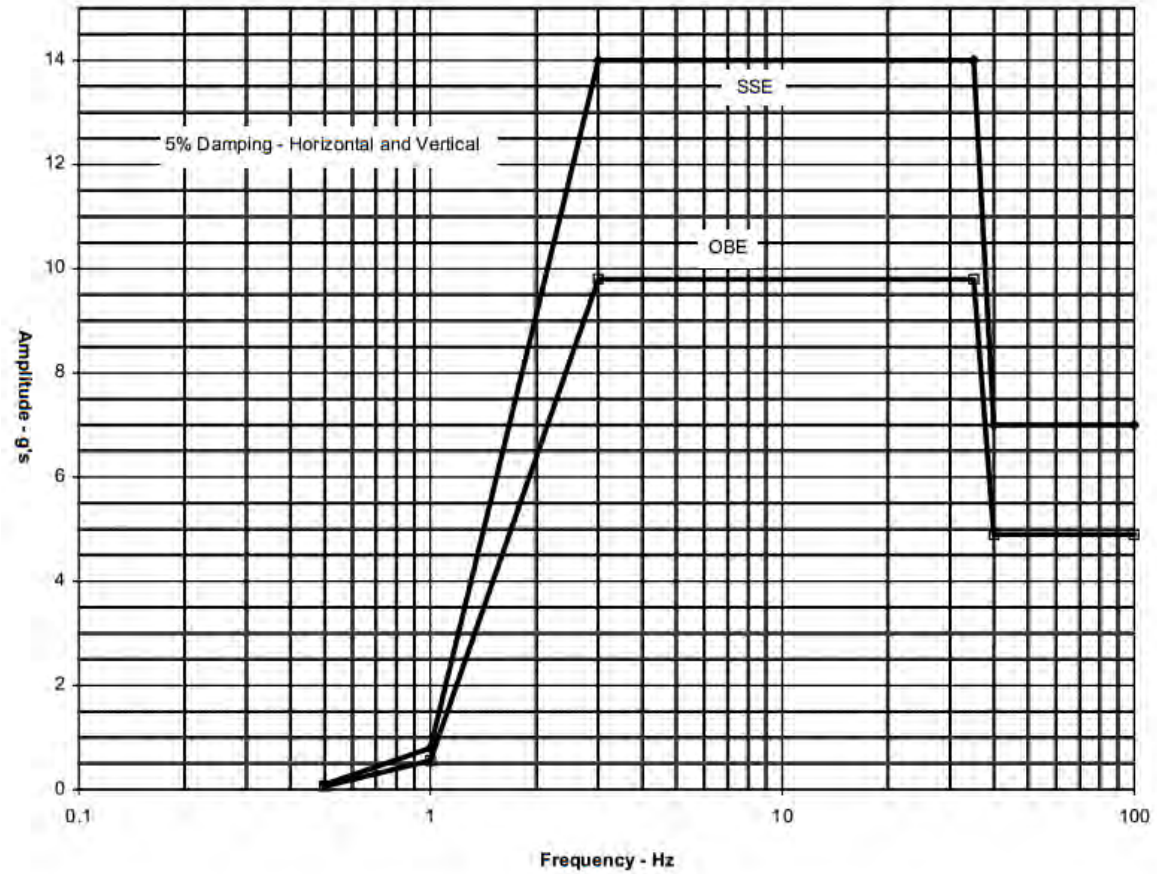
# Test Details: Seismic Test

- Per EPRI TR 107330 Section 4.3.9
- Laboratory test, destructive
  - Requires large hydraulic shake table
  - Causes deformation of cabinet frames
- Category I or II Test Specimen requirements
  - Category I is for safety systems
    - Requires both structural integrity and full unit function through the whole test
  - Category II is for non-safety systems
    - Only requires structural integrity
- Seismic spectrum varies with job site and mounting method
  - EPRI TR 107330 requirement for Class 1E safety systems
  - Bolting vs welding has different damping % requirements
  - Site-specific non-class 1E spectra based on elevation and site data
- Required 10% Margin by IEEE 344



# Test Details: Seismic Test (Continued)

- Class 1E Seismic Spectrum per EPRI TR-107330



## Test Details: Seismic Test (Continued)

- HFC-FPGA Test Specimen mounting
  - Bolted to Test Fixture
  - Test Fixture bolted to triaxial seismic table
  - Accelerometers mounted to representative locations
- Test sequence executed
  - Resonance search
  - 5 OBE
  - 1 SSE
  - Resonance search
- All automated tests running during test sequence
  - Automated Operability Tests
  - Burst of Events Test

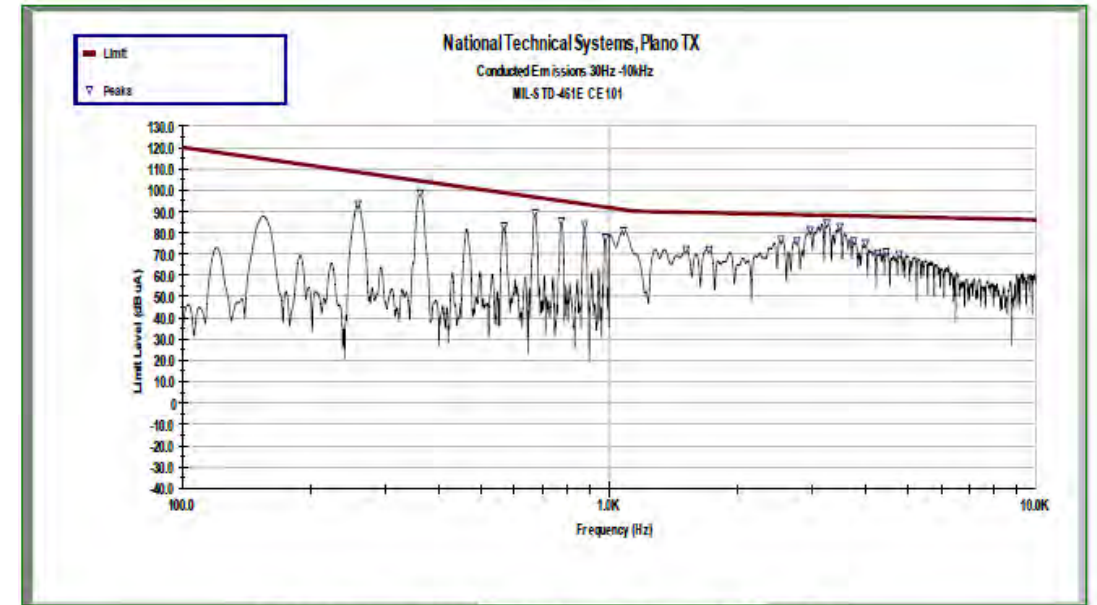


# Test Details: EMI/RFI Test

- Per NRC RG 1.180, MIL-STD-461E
  - These standards have been updated and approved by the USNRC since the latest endorsed revision of EPRI TR 107330
- Laboratory test, potentially destructive testing
  - Anechoic chambers, emitting and receiving antennae
  - Susceptibility tests may damage electronics
- Two categories of tests with multiple ways to fulfill the requirements: MIL-STD or IEC
  - Emissions
    - CE101, CE102, RE101, RE102 from MIL-STD-461E
    - CISPR 11 from IEC 61000-6-4
  - Susceptibility
    - CS101, CS114, CS115, CS116, RS101, RS103 from MIL-STD-461E
    - IEC 61000-4-(3, 4, 5, 6, 8, 9, 10, 12, 13, 16)
- HFC uses MIL-STD testing as a default
  - May be interchanged with the equivalent IEC test(s) when needed per NRC RG 1.180

# Test Details: EMI/RFI Test (CE101)

- Low-frequency conducted emissions
  - 30 Hz to 10 kHz
  - Test performed on line and neutral side
  - Limit set by NRC RG 1.180
- Power is run from a lab-provided source through lab equipment, then to the Test Specimen
  - Capacitors are installed on the incoming power lines to reduce ambient noise
  - Any ferrites or line filters used must be installed in the final production unit
- Potential causes of failure include power supplies and improper grounding
- dB requirements may be relaxed as a function of current
  - $\text{dB relaxation} = 20 \log(\text{fundamental current})$
  - With a fundamental current of 3.5A, relaxation was applied



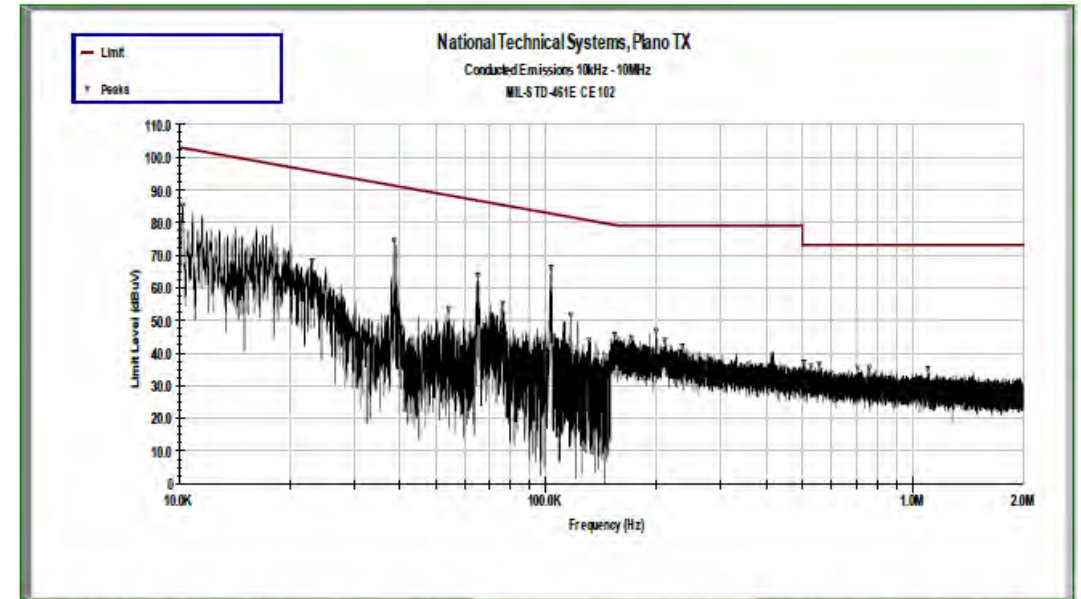
CE101 Conducted Emissions 30Hz – 10 kHz, Line



Line Test Setup for CE101

# Test Details: EMI/RFI Test (CE102)

- High-frequency conducted emissions
  - 10 kHz to 2 MHz
  - Test performed on line and neutral side
  - Limit set by NRC RG 1.180
- Power is run from a lab-provided source through lab equipment, then to the Test Specimen
  - Capacitors are installed on the incoming power lines to reduce ambient noise
  - Any ferrites or line filters used must be installed in the final production unit
- Potential causes of failure include power supplies and improper grounding
- Different emissions limits based on AC Voltage
  - Higher voltage allows for higher limit
  - Partitioned for 28V, 115V, 220V, and 440V
  - 115 VAC used for HFC-FPGA



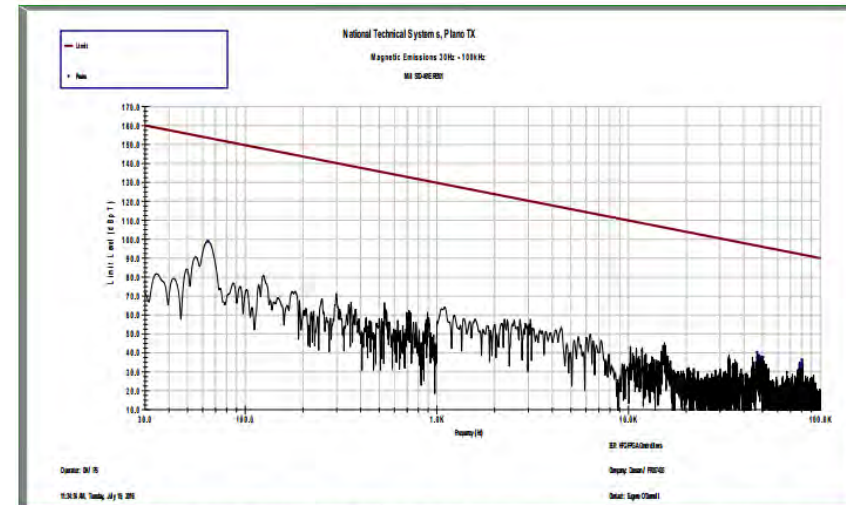
CE102 Conducted Emissions 10 kHz – 10MHz, 230VAC/50Hz Line with Line Filter



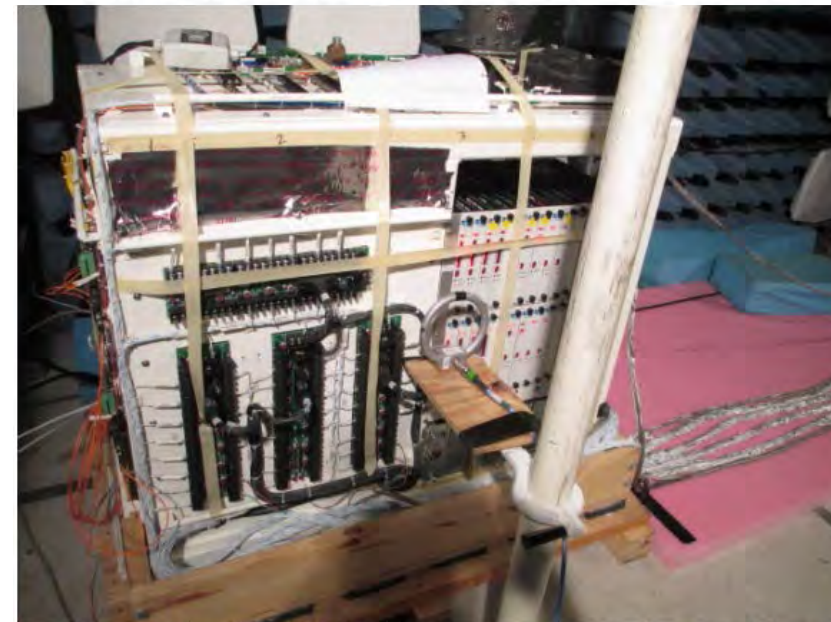
Line Test Setup for CE102

# Test Details: EMI/RFI Test (RE101)

- Radiated emissions, magnetic field
  - 30 Hz to 100 kHz
  - Test performed in a grid around the Test Specimen
  - Limit set by NRC RG 1.180
- Unit is powered on and emissions recorded by an external antenna
  - Measurements are taken 7cm from the surface of the unit
  - May be performed in a worst-case scenario (doors open) as opposed to normal operation (doors closed)
- Potential causes of failure
  - Unshielded power lines
  - Improper grounding
  - Internal components not designed for low-emissions operation



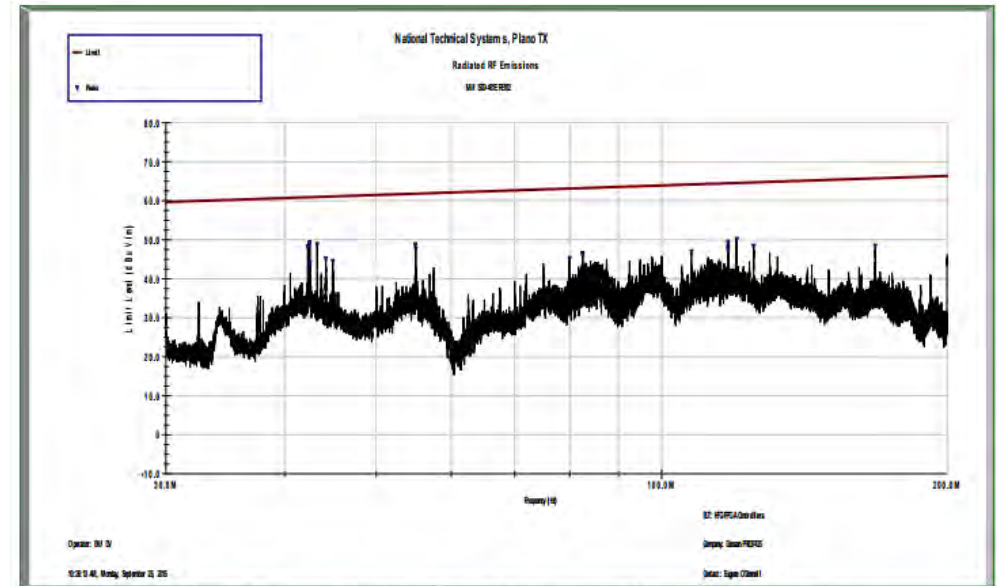
RE101 Magnetic Fields from 30Hz – 100 kHz, Back of the unit, Location B3



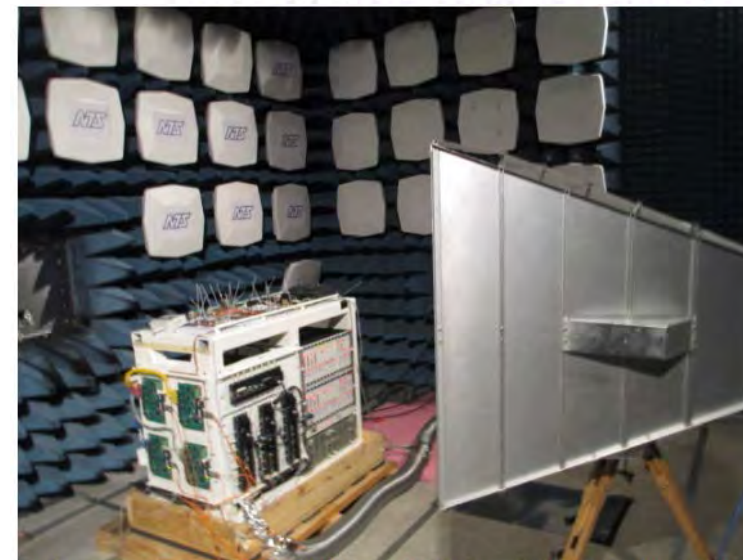
General Test Setup for RE101, Front on the unit, Location B3

# Test Details: EMI/RFI Test (RE102)

- Radiated emissions, electric field
  - 2 MHz to 10 GHz
  - Test performed for vertical and horizontal emissions
  - Partitions into frequency ranges based on lab capabilities
- Unit is powered on and emissions recorded by an external antenna
  - Measurements are taken at a distance of 1m
  - May be performed in a worst-case scenario (doors open) as opposed to normal operation (doors closed)
  - Test cases
    - Bidirectional 2 MHz to 30 MHz
    - Two 30 MHz to 200 MHz
    - Two 200 MHz to 10 GHz
- Potential causes of failure
  - Unshielded power lines
  - Improper grounding
  - Internal components not designed for low-emissions operation
  - Signal coupling in from communication equipment



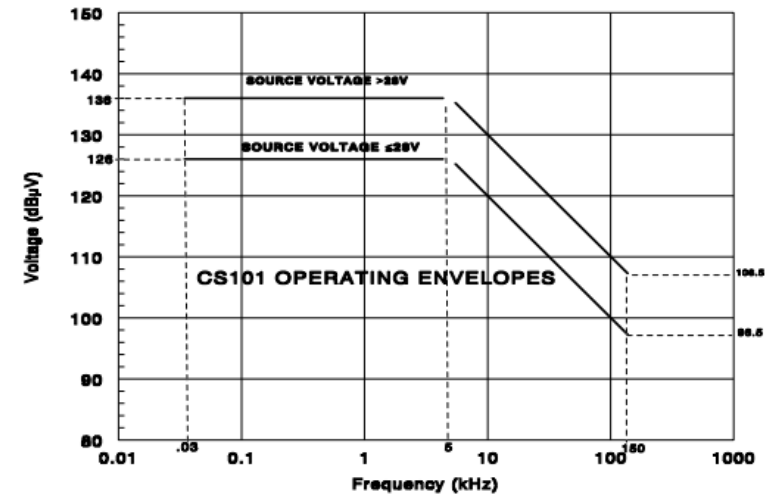
RE102 Electric Fields from 30MHz – 200MHz, Horizontal



General Test Setup for RE102 from 200MHz – 1000MHz, Horizontal

# Test Details: EMI/RFI Test (CS101)

- Conducted susceptibility, low frequency
  - 30 Hz to 150 kHz
  - Performed on AC power leads
- Unit power is routed through a signal generator
  - Signal applied to common power source point
    - Incoming AC power
    - Output of DC power supplies
  - Applied signal strength is as required in NRC RG 1.180
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Fluctuations in power supply outputs
  - Damage to sensitive components

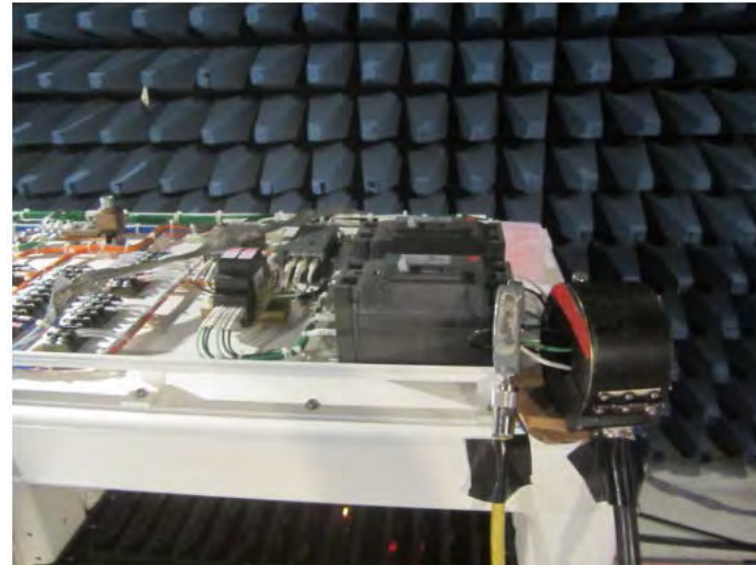


General Test Setup for CS101 120Hz – 150 kHz



## Test Details: EMI/RFI Test (CS114)

- Conducted susceptibility, high frequency
  - 10 kHz to 30 MHz
  - Performed on AC power leads
  - Performed on signal lines
  - Different test levels for signal vs power leads
- Affected lines are run through inducting coils
  - AC and DC power tested separately
  - At least one of each type of signal line (Digital, Analog, C-Link) must be tested
  - Bundles of similar signal cables may be tested
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Fluctuations in power supply outputs
  - Damage to sensitive components
  - Lowered accuracy in analog signals



General Test Setup for CS114 from 10 kHz – 30MHz, Test on AC Bundle



General Test Setup for CS114 from 10 kHz – 30MHz, Test on Signal Bundle 2

## Test Details: EMI/RFI Test (CS115)

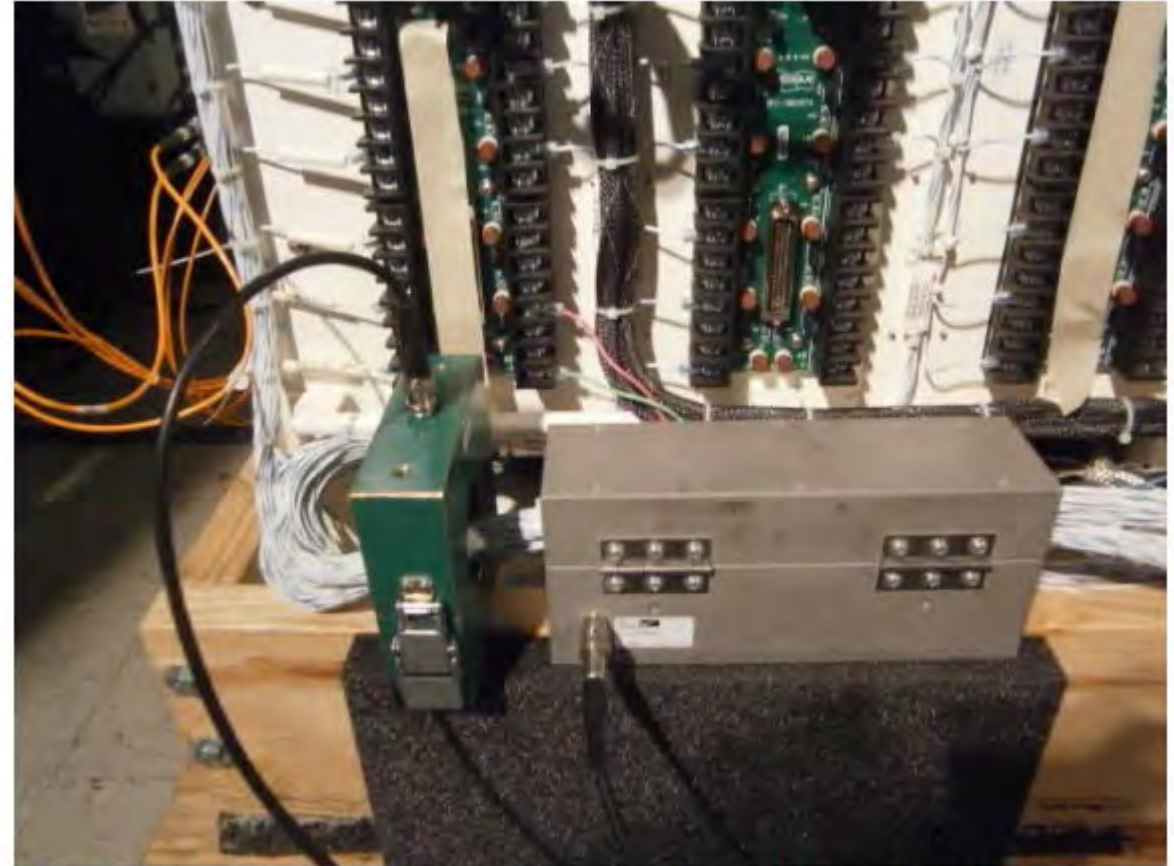
- Conducted susceptibility, bulk cable injection
  - Impulse excitation
  - 2 Amperes
  - Performed on signal lines
- Affected lines are run through inducting coils
  - At least one of each type of signal line (Digital, Analog, C-Link) must be tested
  - Bundles of similar signal cables may be tested
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Fluctuations in power supply outputs
  - Damage to sensitive components
  - Lowered accuracy in analog signals
  - Spurious digital signals



**General Test Setup for CS115 Impulse Excitation on Signal Bundle 1**

## Test Details: EMI/RFI Test (CS116)

- Conducted susceptibility, damped sinusoidal transients
  - 10 kHz to 100 MHz
  - 5 Amperes
  - Performed on signal lines
  - Partitioned into frequency ranges based on lab capability
- Affected lines are run through inducting coils
  - At least one of each type of signal line (Digital, Analog, C-Link) must be tested
  - Bundles of similar signal cables may be tested
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Fluctuations in power supply outputs
  - Damage to sensitive components
  - Lowered accuracy in analog signals
  - Spurious digital signals



**General Test Setup for CS116, Damped Sinusoidal on Signal Bundle 1**

## Test Details: EMI/RFI Test (RS101)

- Radiated susceptibility, magnetic field
  - 30 Hz to 100 kHz
  - Applied magnetic field
  - Performed in a grid pattern over entire Test Specimen
- Antenna induces magnetic field locally
  - Similar to RE101, but susceptibility, not emissions
  - Test area size dependent on lab equipment
  - Entire Test Specimen area must be tested
  - Test duration is relatively long (~40 minutes per square)
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Damage to sensitive components



**Test Setup for RS101, 30Hz – 100 kHz, Front of the EUT, Location B4**

## Test Details: EMI/RFI Test (RS103)

- Radiated susceptibility, electric field
  - 30 MHz to 10 GHz
  - Applied electric field of 10 V/m
  - Performed on front and back face of Test Specimen
- Antenna induces electric field
  - Similar to RE102, but susceptibility, not emissions
  - Vertical and horizontal fields applied
  - Antenna distance of 3 meters
- Potential impacts
  - Communication errors in controllers
  - Equipment resetting
  - Damage to sensitive components
  - Damage to communication equipment



**General Test Setup for RS103 from 8GHz - 10GHz, Vertical Front (right side of the EUT)**

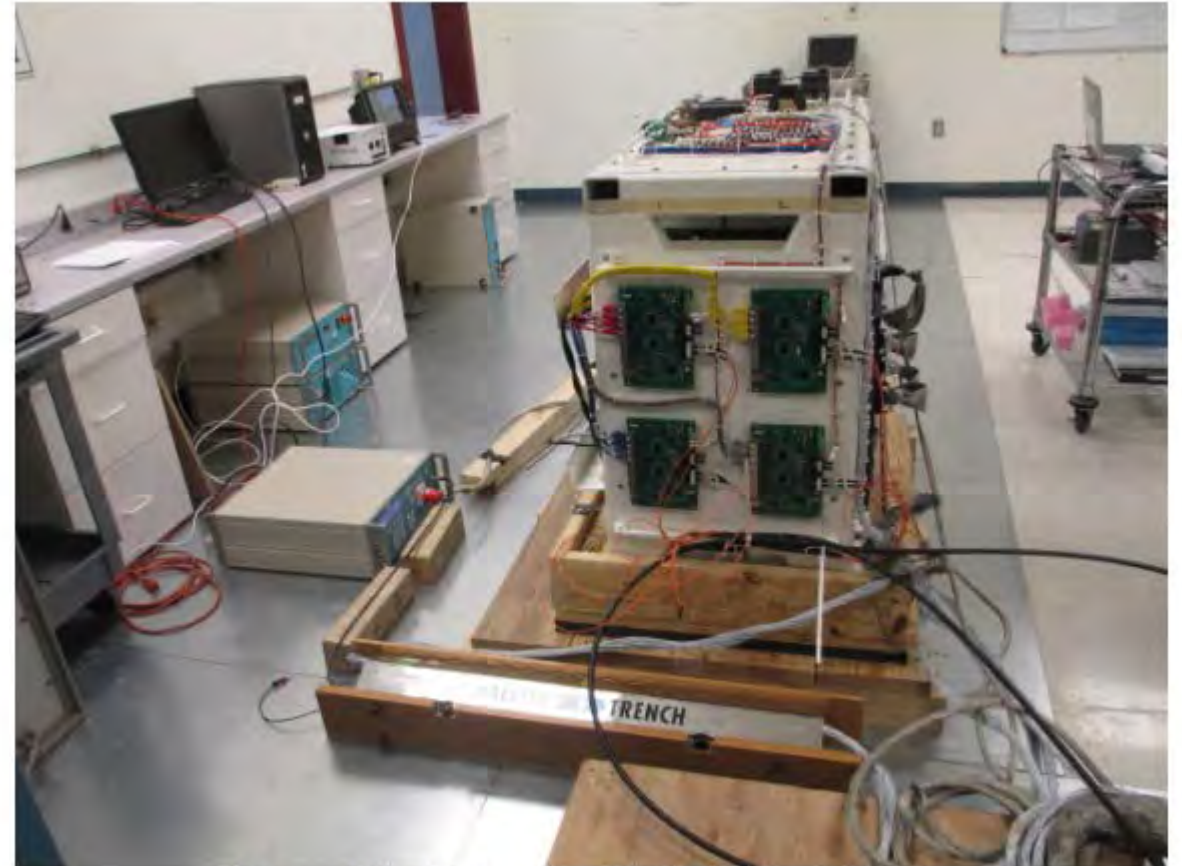
# Test Details: Surge Withstand Test

- Per NRC RG 1.180
- Laboratory testing, potentially destructive test
  - Signal generator
  - Ground plane
  - Surges are applied to the external power leads of the Test Specimen
- Ring wave: IEC 61000-4-12
  - 2 kV and 4 kV exposures
  - Simulates open-circuit voltage waveforms
- Combination wave: IEC 61000-4-5
  - 2 kV / 1 kV and 4 kV / 2 kV exposures
  - Simulates lightning strikes, fuse operation, capacitor switching
- EFT: IEC 61000-4-4
  - 2 kV and 4 kV exposures
  - Simulates load switching in equipment and subsystems
  - Lower-level tests (0.5 kV) performed on signal lines

## Test Details: Surge Withstand Test (Continued)



**General Test Setup for EFT, AC Power Input**



**General Test Setup for EFT, J4 Signal Bundle**

# Lessons Learned

- Operability and Prudency Testing
  - Clear definition of what tests can and cannot be run during EQ testing
  - Automated data processing tools assist in generating results from months of data
  - Automated data logging tools need a high enough resolution to capture incorrect transitions
- Environmental Testing
  - Keep potential replacement cards on site
  - Have a plan for quick access to potential boards, especially during high heat test.
  - Include margins in test profile submitted to laboratory



# Lessons Learned

- EMI/RFI
  - Use communication equipment that will pass EMI/RFI when possible
  - Select line filters and to include in test specimen specific to both the measured ranges, and known oscillator frequencies on modules
  - Verify all module bezels are secured in to the proper torque values, for the sake of proper grounding
- Seismic
  - Design all parts of the Test Specimen to endure the worst-case SSE
  - Check and re-check all connectors for tightness
  - Carefully check for damage between OBEs

# Lessons Learned



Figure 1 - Environmental Stress Test

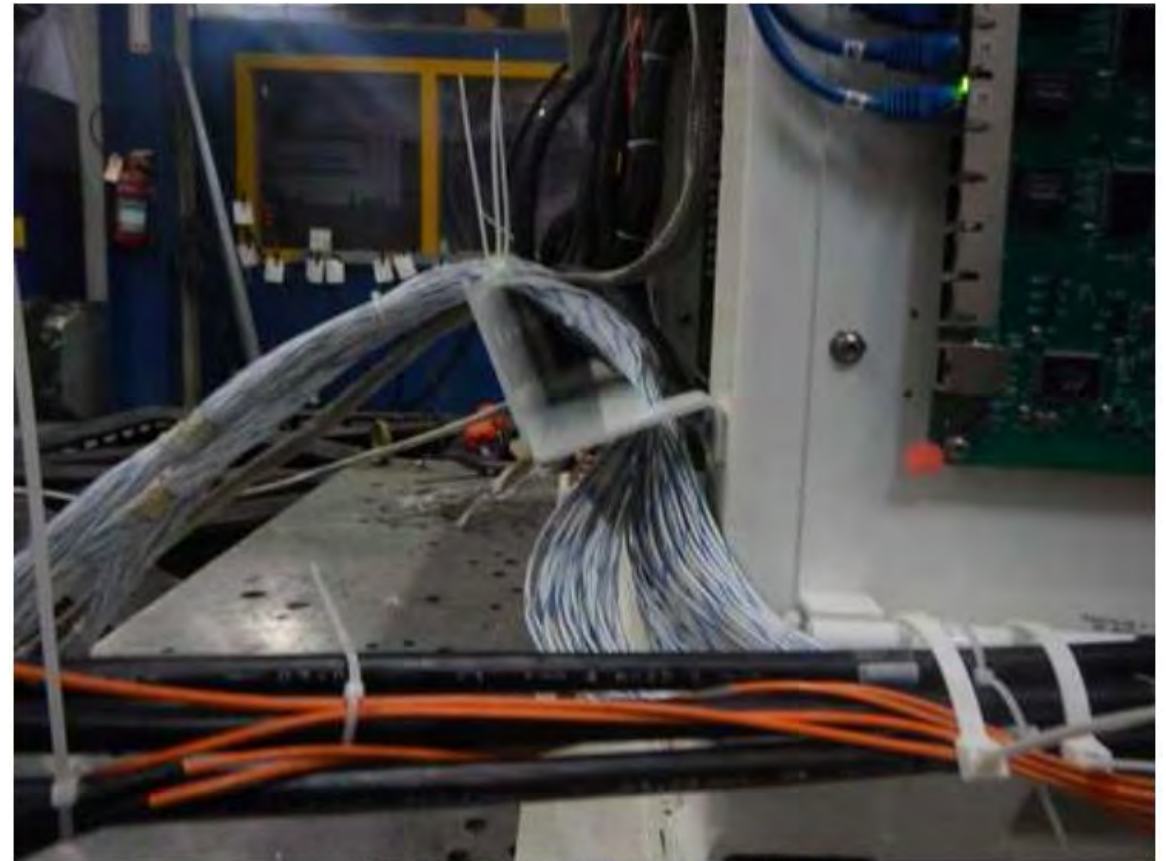


Figure 22 - Seismic Test - Post-Test

# Questions?