

11th International Workshop on Application of Field Programmable Gate Arrays in Nuclear Power Plants October 8-11, 2018 in Dallas, Texas

Introduction of Class 1 FPGA Platform vCOSS S-zero for the UK ABWR

Junichi Kumagai Toru Motoya Hitachi, Ltd.

© Hitachi-GE Nuclear Energy, Ltd., Hitachi, Ltd. 2018. All rights reserved.



- 1. About Hitachi and Hitachi's C&I
- 2. UK ABWR Project Overview
- 3. UK ABWR C&I System Architecture
- 4. Class 1 FPGA Platform



- 1. About Hitachi and Hitachi's C&I
- 2. UK ABWR Project Overview
- 3. UK ABWR C&I System Architecture
- 4. Class 1 FPGA Platform

About Hitachi, Ltd. (FY2017)

HITACHI Inspire the Next



Global Expansion* (FY2017)

HITACHI Inspire the Next



Japan	Revenues: \$ 42.4 billion/Number of companies: 202/Number of employees: 168 thousand
Outside Japan	Revenues: \$ 43.1 billion/Number of companies: 677 /Number of employees: 139 thousand
Total	Revenues: \$ 85.5 billion/Number of companies: 879/Number of employees: 307 thousand

* Revenues: FY2017, Number of companies and employees: As of end of FY2017 © Hitachi-GE Nuclear Energy, Ltd., Hitachi, Ltd. 2018. All rights reserved.





DCS: Distributed Control System Note: Definition of Safety System and Safety Related System is based on IAEA Safety Glossary 2007

© Hitachi-GE Nuclear Energy, Ltd., Hitachi, Ltd. 2018. All rights reserved. 5







- 1. About Hitachi and Hitachi's C&I
- 2. UK ABWR Project Overview
- 3. UK ABWR C&I System Architecture
- 4. Class 1 FPGA Platform

- Horizon Nuclear Power is planning to build 1,350 MWe class Advanced Boiling Water Reactors (ABWR) in Wylfa and Oldbury.
- The primary focus is to secure all key agreements and permissions in place for the Final Investment Decision in 2019.
- Commercial operation of the 1st unit at Wylfa is planned to be in the middle 2020s.



- Hitachi-GE Nuclear Energy as an ABWR supplier, officially applied Generic Design Assessment (GDA) licensing process to the UK regulator in 2013.
- Final process of Step-4 was completed in December 2017.
- Currently at pre-engineering phase.



[News Release] http://www.hitachi.com/New/cnews/month/2017/12/171214.html



- 1. About Hitachi and Hitachi's C&I
- 2. UK ABWR Project Overview
- 3. UK ABWR C&I System Architecture
- 4. Class 1 FPGA Platform

UK regulatory expectations for C&I are;

- Complying with International Code and Standards such as IEC 61513
- Referring to assessment guides such as SAP, TAGs
- Referring to relevant good practice such as feedbacks from other GDA

Based on the above expectations, Design features of UK ABWR system are determined, such as;

- System reliability according to Category & Class
- Redundancy
- Separation
- Diversity

SAP: Safety Assessment Principle TAG: Technical Assessment Guide IEC: International Electro technical Commission



















- 1. About Hitachi and Hitachi's C&I
- 2. UK ABWR Project Overview
- 3. UK ABWR C&I System Architecture
- 4. Class 1 FPGA Platform



Hitachi developed a Class 1 Platform VCOSS S-zero

The main features are:

- Each module has FPGAs inside and connected to safety field bus.
- Development process complies with IEC 61513, 62566, 61508 and 62443
- Without processor, firmware, OS, middleware
- Supporting floating-point arithmetic without FPGA vendor's floating-point IP cores



Reliability requirement assigned to SSLC is 10^{-4} [PFD]. The platform is required IEC 61508 SIL 3 as single configuration in order to satisfying 10^{-4} PFD as a whole system.



Certified as following from TÜV Rheinland in Jan. 2018.

- vCOSS S-zero complies with IEC 61508 SIL 3 as single configuration.
- Measures for fault avoidance is applied in accordance with IEC 61508 SIL 4.
- Furthermore, Certified as SL 1 (Cyber Security Standard) IEC 62443-4-1:2018 (Edition 1.0), IEC 62443-4-2:2017 (65/663/CDV)

SSLC: Safety System Logic and Control system PFD: Probability of Failure on Demand





Design and Development process for SIL 4

Calculation Macros



The figure focuses on the range of the FPGA bit stream from the specification.

нітасні

Inspire the Next

Design and Development process for SIL 4

Calculation Macros



We applied the formal verification to the files generated from the specification to comply with SIL 4.

нітасні

Inspire the Next

© Hitachi-GE Nuclear Energy, Ltd., Hitachi, Ltd. 2018. All rights reserved. 21



- Allow user to design as function block diagram using general design tool
- Support wide variety macros which are developed as white-box

Calculation Macros



Hitachi completed GDA on schedule without GDA issues including C&I field.

Our design features

- Different Platforms are adopted to achieve the diversity.
- Developed vCOSS S-zero in accordance with IEC 61513 series.
- **vCOSS S-zero** has been certified for single SIL 3 according to IEC 61508.

Furthermore, the certificate confirmed that measures for fault avoidance is applied in accordance with IEC 61508 SIL 4.

 vCOSS S-zero has also been certified for Security Level 1 according to IEC 62443-4.



END

Introduction of Class 1 FPGA Platform vCOSS S-zero for the UK ABWR

Junichi Kumagai Toru Motoya

Hitachi, Ltd.

HITACHI Inspire the Next