

HFC-6000 FPGA Platform

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Innovation Leadership Service

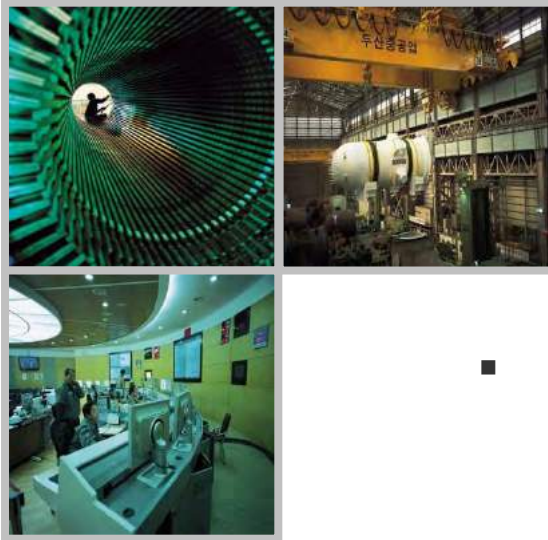


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HFC I&C DEVELOPMENT

- **HFC-6000 PLATFORM IS A COMBINATION OF ADVANCED MICROPROCESSORS, DSP, AND FPGA**
 - RECEIVED US NRC SE REPORT IN APRIL, 2011 AND TUV SIL3 IN 2010/2013/2018
- **HFC-FPGA PLATFORM IS SUITABLE FOR SOME SAFETY CONTROL APPLICATIONS IN NUCLEAR POWER PLANT DUE TO THE DETERMINISTIC NATURE OF FPGA FSM BASED DESIGNS**
- **THE DEVELOPMENT OF A GENERIC FPGA SAFETY I&C PLATFORM DEPENDS UPON THE MATURITY AND ENHANCEMENT OF FPGA TECHNOLOGY IN ORDER TO IMPROVE THE CALCULATION DENSITY AND NETWORKING CAPABILITY.**
- **HFC TREATS FPGA DESIGNS AS A MIX OF SOFTWARE AND HARDWARE**
 - DEVELOPMENT FOR FPGA APPLICATIONS FOLLOWS SYSTEM, SOFTWARE, AND HARDWARE DEVELOPMENT LIFECYCLE PROCESSES.
- **DEVELOPMENT GOALS AND OBJECTIVES**
 - HFC 'S GENERIC FPGA NUCLEAR SAFETY I&C PLATFORM IS BASED UPON THE FOUNDATION OF CURRENT HFC-6000 TECHNOLOGY.
 - HFC HAS FILED FPGA HFC-6000 DESIGN AS AN AMENDMENT TO CURRENT SER.
 - TO ACQUIRE US NRC SE REPORT FOR THE HFC-6000 FPGA AMENDMENT .

REGULATORY GUIDANCE AND INDUSTRY STDS

- **THE NUREG/CR-7006 IS THE CURRENT NRC REGULATORY GUIDANCE FOR THE FPGA.**
- **OTHER APPLICABLE REGULATORY GUIDANCE AND INDUSTRY STANDARDS INCLUDE**
 - NUREG-0800 BTP 7-14,
 - NRC RG 1.152, 1.168, 1.169, 1.170, 1.171, 1.172, 1.173
 - DO-254 (DESIGN ASSURANCE),
 - IEEE STD 603
 - IEEE STD 1012-2004 AND 2012 (V&V),
 - IEC 61508 (FUNCTIONAL SAFETY - TUV)
 - IEEE STD 7-4.3.2 (SAFETY DIGITAL SYSTEMS).
- **THE INTENT OF HFC'S FPGA DESIGN AND DEVELOPMENT PROCESS IS TO MEET RELEVANT REGULATORY REQUIREMENTS AND INDUSTRY STANDARDS.**

HFC-6000 PLATFORM

HFC-6000



Features

- Nuclear safety class 1E qualified
- Modular Packaging (19"/23" Rack)
- Redundant and Triple Redundant
- DCS and Loop application
- Dedicated CSM & M/A stations
- Nuclear qualified Flat Panel Display
- Superior Response time
- Thousands controllers installed in Nuclear Power Plants

Application

- Nuclear Power Plant Safety
- Turbine Control
- Mission Critical Control
- TÜV SIL-3 Certified



• HFC-FPGA I&C SYSTEM TO USE THESE HFC-6000 SAFETY QUALIFIED FEATURES

– MECHANICAL

- CARD FORM FACTOR, 19 INCH 5U CHASSIS, FIELD CONNECTIVITY, SEISMIC CHASSIS/CABINET

– ELECTRICAL – REDUNDANT POWER AND COMMUNICATION INTERFACES

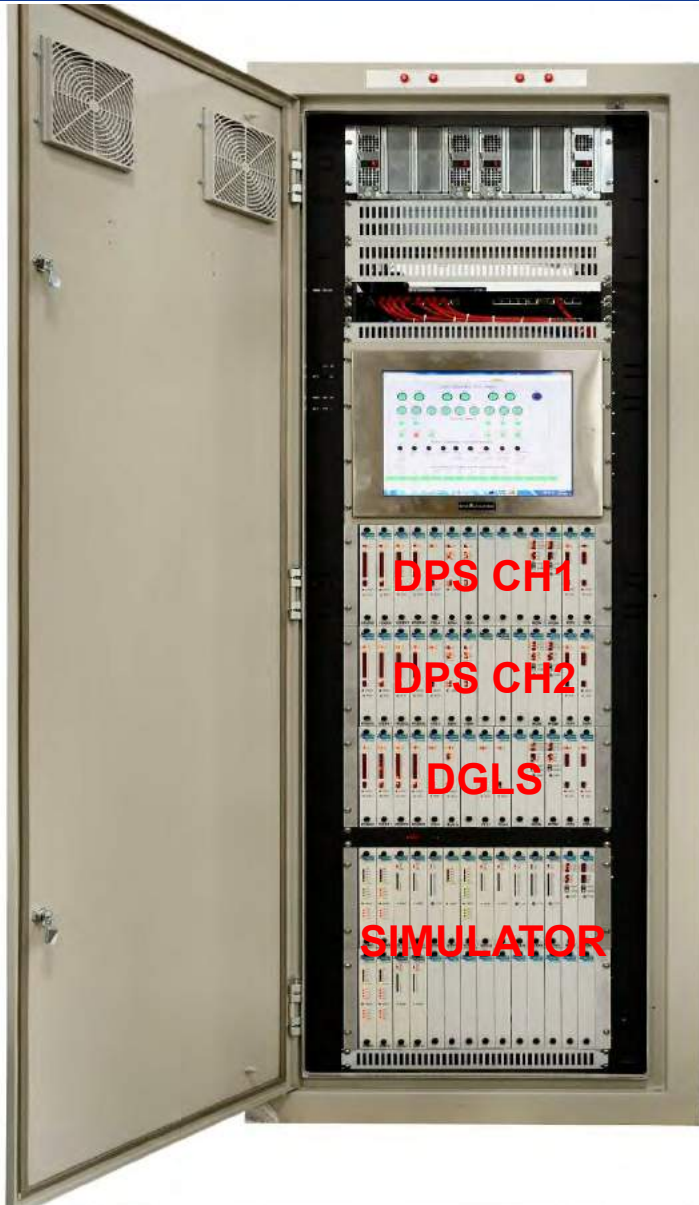
– APPLICATION DEVELOPMENT

- SHARES HFC-6000 TOOLS FOR DEVELOPING APPLICATIONS AND HMI GRAPHICS

– REDUNDANCY – CENTRALIZED CONTROLLER TO IMPLEMENT REDUNDANCY

– I/O MODULE LINEUP – MICROPROCESSOR I/O MODULES AVAILABLE IN FPGA IMPLEMENTATIONS

Typical FPGA HFC-6000 EQ Cabinet



- ✓ HFC's nuclear safety class cabinet
- ✓ Three(3) racks of FPGA PCB modules for typical parameterized safety and protection functions; the Test Specimen Application Program (TSAP) includes the following:
 - Functional Diesel Generator Load Sequencer
 - Functional Diverse Protection System (DPS) – 2 Ch
- ✓ 5U Racks – up to 8 per cabinet
- ✓ Termination boards, Connection cards, cables
- ✓ A rack mounted Personal Computer (PC) with Flat Panel Device (FPD) and Human Machine Interface (HMI) utility software
- ✓ Network Hubs and Fans
- ✓ Rack mounted power supply set - 40ms withhold time, 24VDC
- ✓ Power distribution and a set of circuit breakers

HFC-6000 EVOLUTION TO HFC-FPGA

- **DUAL FPGA ARCHITECTURE REPLACES THE MICROPROCESSOR FOR CONTROL**
 - **CONTROL FPGA** – F-LINK TX/RX TO COMMUNICATE WITH OTHER CARDS IN THE RACK
 - MAIN APPLICATION/PROCESSING ELEMENT DOING APPLICATION AND/OR I/O PROCESSING
 - **DIAGNOSTIC FPGA** – F-LINK RX VERIFIES ACTIVITY AND PROCESSING RESULTS OF THE CONTROL FPGA
 - DISABLES CONTROL FPGA WHEN A FAULT IS DETECTED
 - FAULTS CAN BE HARDWARE OR APPLICATION/I/O PROCESSING RELATED
 - FPGAS COMMUNICATE STATUS AND PROCESSING RESULTS OVER A INTRA-FPGA DATA BUS
 - EXCHANGE HEART BEAT MESSAGES TO VERIFY HEALTH
 - CONTROL FPGA MONITORS FOR POWER FAULTS IN THE DIAGNOSTIC FPGA AND VICE VERSA
 - EACH FPGA HAS APPLICATION DATA STORED IN A NON VOLATILE MEMORY
 - READ AT POWER UP AND USED TO INITIALIZE I/O AND CONTROLLER CARD FPGA MEMORIES
- **ALL C CODE CONTROL FUNCTIONS REPLACED WITH FPGA FSM BASED PROCESSES**
 - HFC HAS A LARGE LIBRARY OF C FUNCTIONS THAT CAN BE IMPLEMENTED IN THE HFC-FPGA SYSTEM

HFC-FPGA SYSTEM DESCRIPTION

- **TWO ARCHITECTURE OPTIONS FOR THE HFC-FPGA SYSTEM**

- DISTRIBUTED – NO CENTRALIZED CONTROLLER, EACH I/O CARD DOES APPLICATION PROCESSING
 - I/O CARDS (FPU) EXCHANGE POINT INFORMATION DIRECTLY
 - FILTERING ELIMINATES UNDESIRE VALUES
 - APPLICATION DISTRIBUTED, FPU RUN PORTIONS OF THE APPLICATION
- CENTRALIZED – APPLICATION PROCESSING IN THE FCPUX ONLY
 - I/O CARDS (FPU) DO MINIMAL PROCESSING AND SEND/RECEIVE RESULTS TO/FROM THE CONTROLLER

- **FPGA NODE – 1 TO 2 RACKS**

- EACH RACK CAN CONTAIN UP TO 14 CARDS (FPU I/O, FPGA CONTROLLERS, OR GATEWAYS)
- RACKS ARE INTERCONNECTED WITH RS-485 CABLING (EXTENSION OF F-LINK)
- FPGA LINK (F-LINK) IS A TOKEN PASSING PROTOCOL
 - OPERATES WITHIN THE FPGA NODE WITH A PERIOD OF 6.8 MSEC.
 - SUPPORTS UP TO 26 FPGA PROCESSING UNITS AND 2 CONTROLLERS

HFC-FPGA SYSTEM DESCRIPTION

- **FPGA PROCESSING UNITS (FPU)**

- CAPABLE OF HANDLING BOTH DIGITAL AND ANALOG ALGORITHMS.
- CONFIGURED AS SINGLE, REDUNDANT OR TRIPLE MODULAR REDUNDANT (TMR) SET.
- COMMUNICATE WITH OTHER FPU AND CONTROLLERS VIA REDUNDANT F-LINK
 - TOKEN-PASSING PROTOCOL (SIMILAR TO HFC'S QUALIFIED C-LINK PROTOCOL)
 - 12.5 MBPS LINK ALLOWS FPUS TO EXCHANGE THEIR I/O STATUS AND INTERNAL DATABASE

- **FPGA CONTROLLER PROCESSING UNIT (FCPUX)**

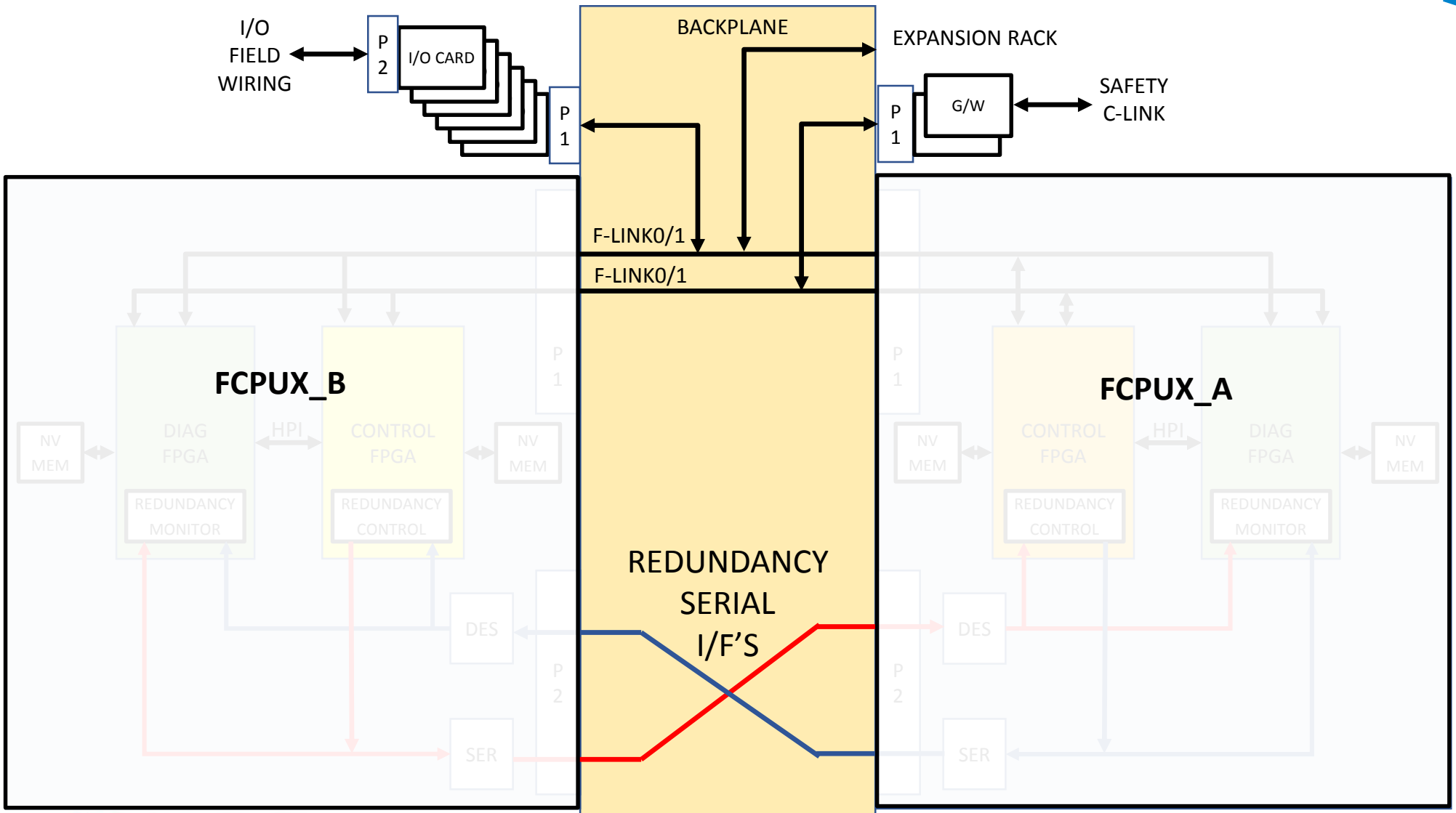
- FPGA BASED CONTROLLER CENTRALIZES APPLICATION IN ONE MODULE
- CAN BE USED IN REDUNDANT CONFIGURATIONS
- PERFORMS ANALOG AND DIGITAL PROCESSING ON INPUT FPU DATA
- COMMUNICATES APPLICATION RESULTS TO OUTPUT FPU
- COMMUNICATES APPLICATION STATUS WITH THE FPGA GATEWAY
 - USES A PRIVATE LINK TO THE GATEWAY CALLED G-LINK
- FCPU – REDUCED CAPACITY FPGA CONTROLLER PROCESSOR UNIT WITH ONBOARD DI/DO

HFC-FPGA SYSTEM DESCRIPTION

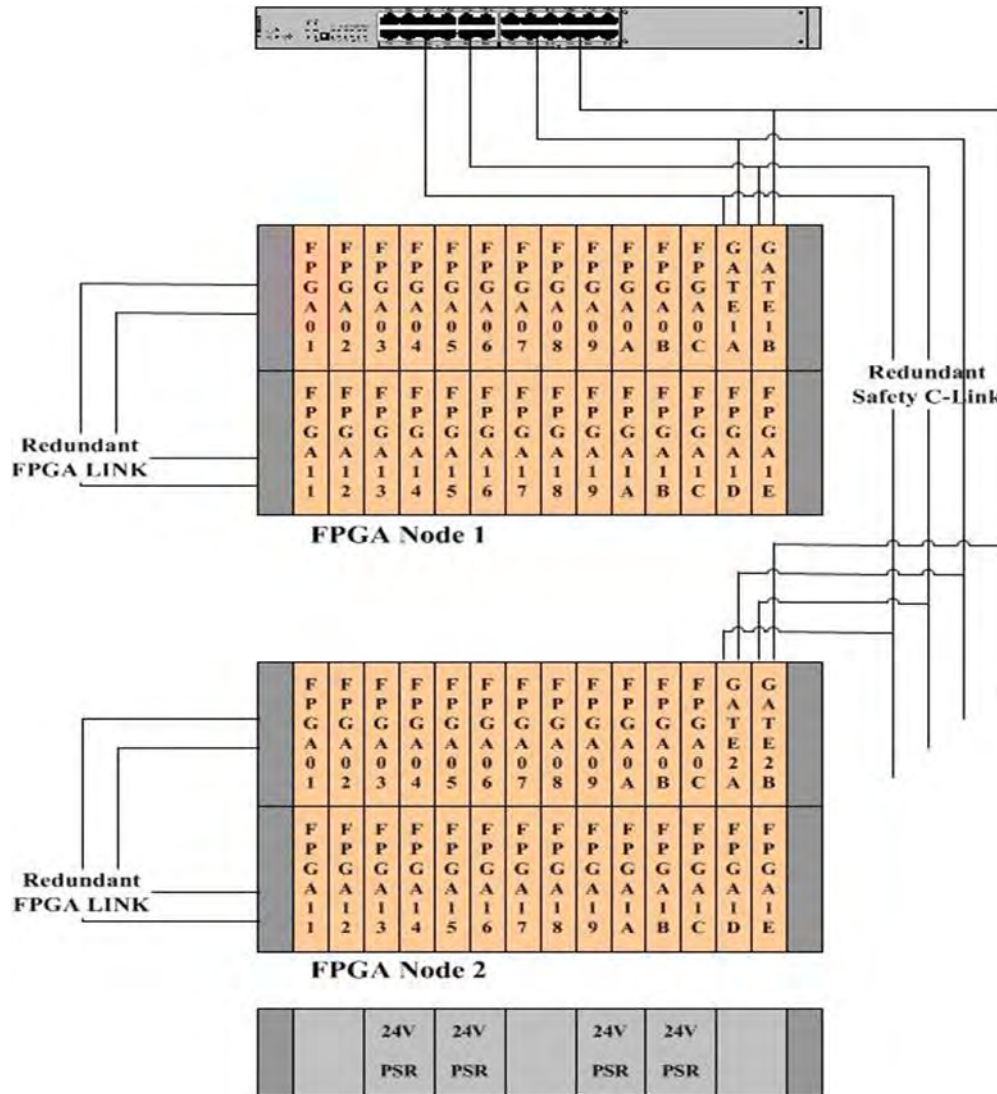
- **FPGA GATEWAY**

- TERMINATES G-LINK DATA FROM FPGA CONTROLLER
- RE-BROADCASTS CONTROLLER DATA USING THE QUALIFIED ETHERNET BASED C-LINK PROTOCOL
- CAN BE USED IN REDUNDANT CONFIGURATIONS

HFC-FPGA COMMUNICATION INTERFACES



HFC-FPGA DISTRIBUTED SYSTEM CONFIGURATION

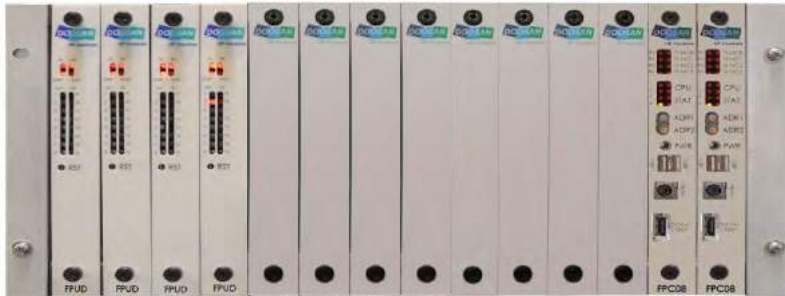


Typical HFC-FPGA system configuration that implements a control system in a **Distributed Loop Control Scheme**

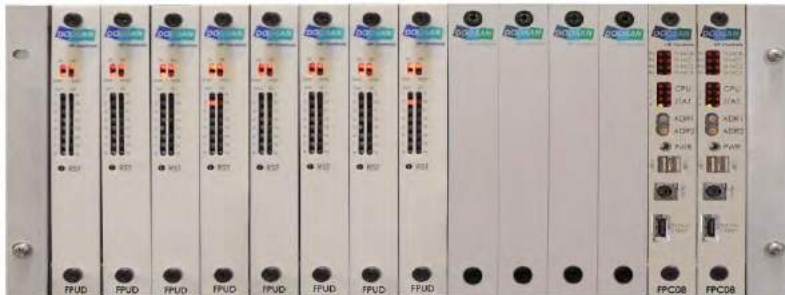
- Two (2) or more FPU I/O Modules and redundant Gateway Controller communicate with:
 - Safety C-Link to other FPGA Nodes
 - F-Link within the FPGA Node
- Each HFC-6000 FPGA Node is capable of connecting up to 26 FPU Control Modules in two (2) racks. All FPU are connected via 12.5MBPS F-Link.
- Accessories (i.e. Power Supply, Hubs,...)

REDUNDANCY IN A DISTRIBUTED ARCHITECTURE

Non-Redundant



Redundant



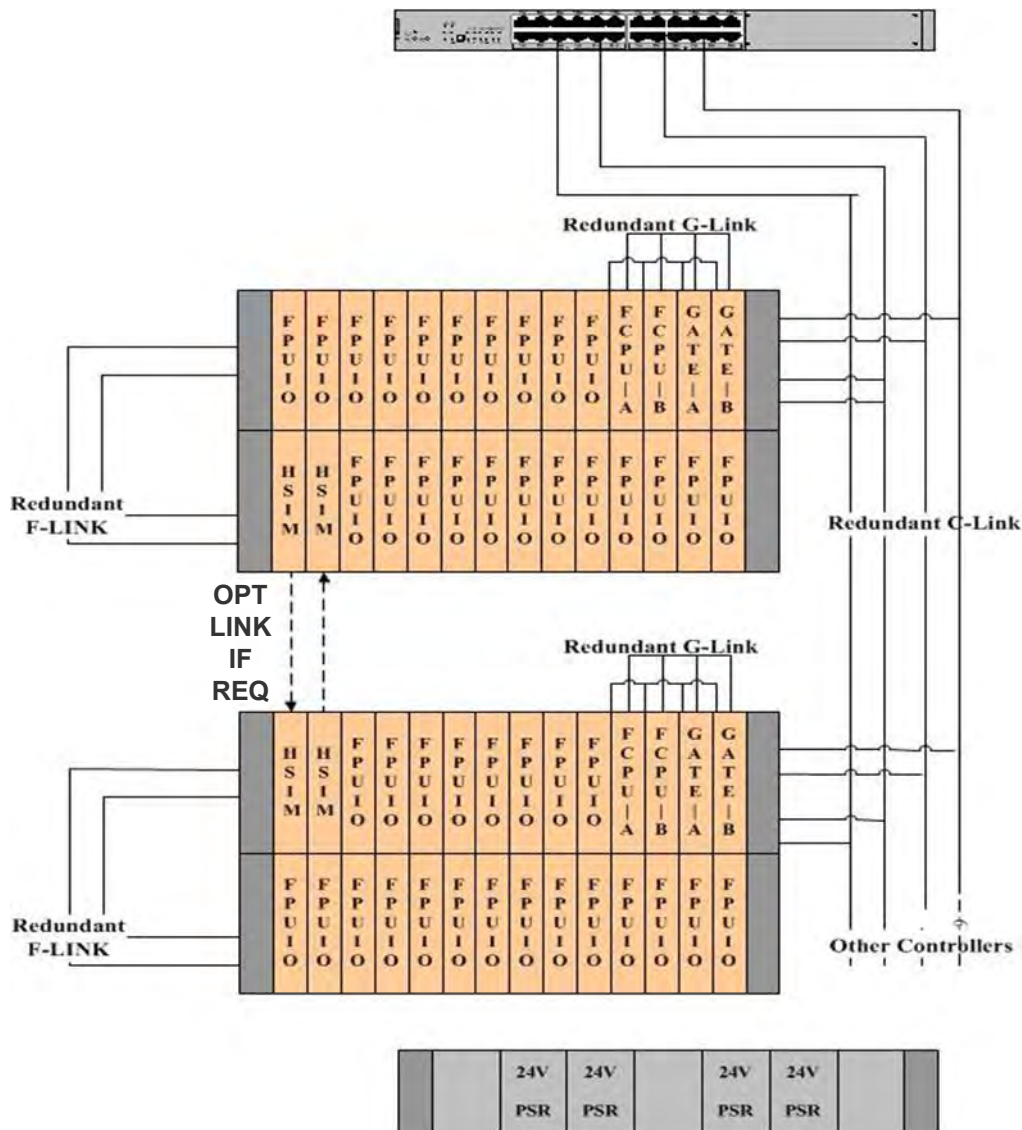
Triple Redundant



This diagram illustrates the system configuration of HFC-6000 FPGA Load Sequencer for NPP application -

- The Load Sequencer logic for NPP can be programed into four (4) HFC-6000 FPGA Processing Units.
- The system can be configured in one of following cases:
 - ✓ *Non-Redundant*
 - ✓ *Dual Modular Redundant (DMR) with 1oo2D voting*
 - ✓ *Triple Modular Redundant (TMR) with 2oo3D voting*
- Voting in DMR and TMR on input signals, controller execution and output signals.

HFC-FPGA CENTRALIZED SYSTEM CONFIGURATION



Typical HFC-FPGA system configuration that implements a control system in a **Centralized Control Scheme**

- Redundant FCPUX and its FPU I/O Modules with redundant Gateway Controller with:
 - Safety C-Link to other controllers
 - G-Link to Gateway Controller
 - F-Link to its FPU I/O Modules
- Each redundant FCPU is capable of connecting up to 24 FPU I/O Modules in two (2) racks via 12.5MB F-Link.
- Accessories (i.e. Power Supply, Hubs,...)

HFC-FPGA I/O AND CONTROLLER CARD LINEUP

- **HFC-FCPUX – FPGA CONTROL PROCESSOR UNIT – USED ONLY IN CENTRALIZED CONTROL SYSTEM**
 - APPLICATION PROCESSOR CONTROL MODULE USING DATA RECEIVED FROM SYSTEM I/O CARDS
 - REDUNDANCY INTERFACE TO MATE FCPUX
 - SUPPORTS REDUNDANCY OVER REDUNDANCY INTERFACE
 - SEPARATE G-LINK INTERFACE TO EWS GATEWAY CARDS
- **HFC-FPUD – FPGA PROCESSOR UNIT – DIGITAL TYPE**
 - FPUD01 – FPUD I/O CARD WITH 16 CHANNELS DI (COMMON OR ISOLATED) AND 16 CHANNELS DO (C-FORM RELAY)
 - FPUD02 – FPUD I/O CARD WITH 32 CHANNELS DI (COMMON OR ISOLATED MODE)
- **HFC-FPUA – FPGA PROCESSOR UNIT – ANALOG TYPE (COMMON OR ISOLATED MODE)**
 - FPUA01 – FPUA ANALOG I/O CARD WITH 16 CHANNELS AI – 4 TO 20 MA
 - FPUA02 – FPUA ANALOG I/O CARD WITH 16 CHANNELS AI – 0 TO 10 V

HFC-FPGA I/O AND CONTROLLER CARD LINEUP

- **HFC-FPUAO – FPGA PROCESSOR UNIT – ANALOG OUTPUT TYPE**
 - FPUAO01 – FPUAO ANALOG I/O CARD WITH 8 CHANNELS AO – 4 TO 20 MA
 - FPUAO02 – FPUAO ANALOG I/O CARD WITH 8 CHANNELS AO – 0 TO 10 V
- **HFC-FPUM – FPGA PROCESSOR UNIT – M TYPE (SUPPORTS 3 RANGES TO 200 C AND 2000 OHM RTD)**
 - ANALOG I/O CARD WITH 8 CHANNELS OF TYPE M 100 OHM PLATINUM RTD INPUTS
- **HFC-FPUL – FPGA PROCESSOR UNIT – E TYPE (SUPPORTS 3 RANGES TO 500 C)**
 - ANALOG I/O CARD WITH 8 CHANNELS OF TYPE E THERMOCOUPLE INPUTS
- **HFC-HSIM – HIGH SPEED INTERFACE MODULE**
 - FPGA BASED INTRA-SAFETY SYSTEM FIBER OPTIC COMMUNICATION LINK
 - 2 OPTICAL CHANNELS CONFIGURABLE AS EITHER TRANSMIT OR RECEIVE

HFC-FPU FPGA Based I/O Modules

HFC-FPU DI/DO/AI/AO/RTD/TC

Product Features

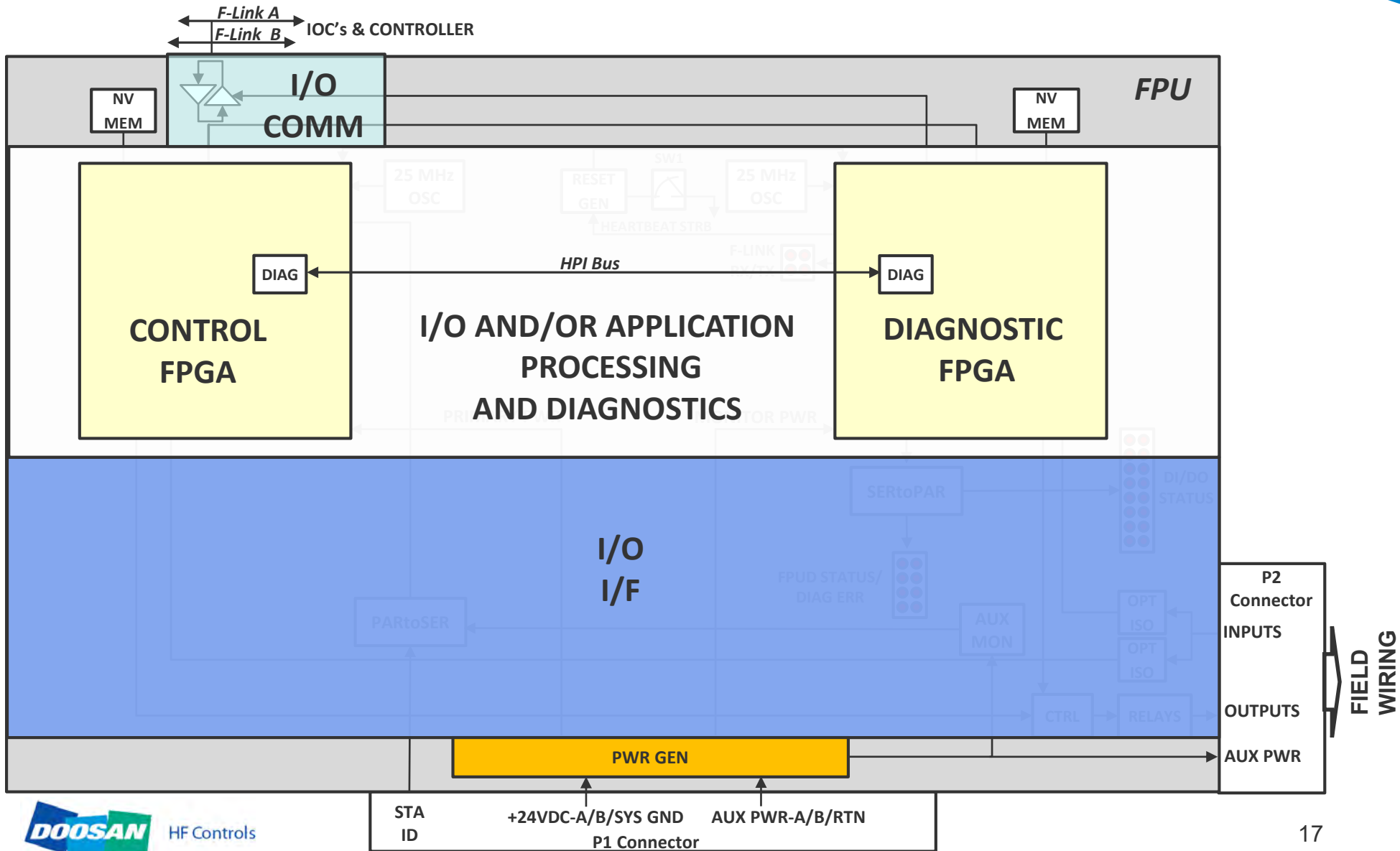
- ❖ FPGA based intelligent module diagnostics and self checking capabilities
- ❖ Power on reset circuitry with onboard watchdog timer
- ❖ Redundant power feeds with onboard diode auctioneering and fuse protection
- ❖ Redundant communications interfaces
- ❖ Onboard status LED indications

Functional Description

- ✓ All HFC-FPU are FPGA based intelligent I/O modules to perform these functions: sampling of input data and/or transmit to FCPUX or receive output data from the FCPUX and drive output devices.
- ✓ The two FPGAs on the HFC-FPU I/O modules are the Control FPGA and Diagnostic FPGA. They are intended to work in tandem, processing the same input and/or output data and comparing the results to detect faults.
- ✓ The dual FPGA structure is designed to protect final output data from Single Event Upset and single component failure that may impact safety function.
- ✓ The HFC-FPU circuit structure includes multiple layers of safety function protection circuitry/logic to enforce the I/O channel verification and communication data acquisition/verification.
- ✓ The diagnostic FPGA controls the F-Link RS485 transmit enable signal. The diagnostic FPGA also monitors all I/O activities. For any diagnostic non-conformance, the diagnostic FPGA can invalidate the FPU function or mark channel data as questionable



FPU (FPGA PROCESSOR UNIT) BLOCK DIAGRAM



HFC-FCPUX FPGA SYSTEM CONTROLLER

Product Features

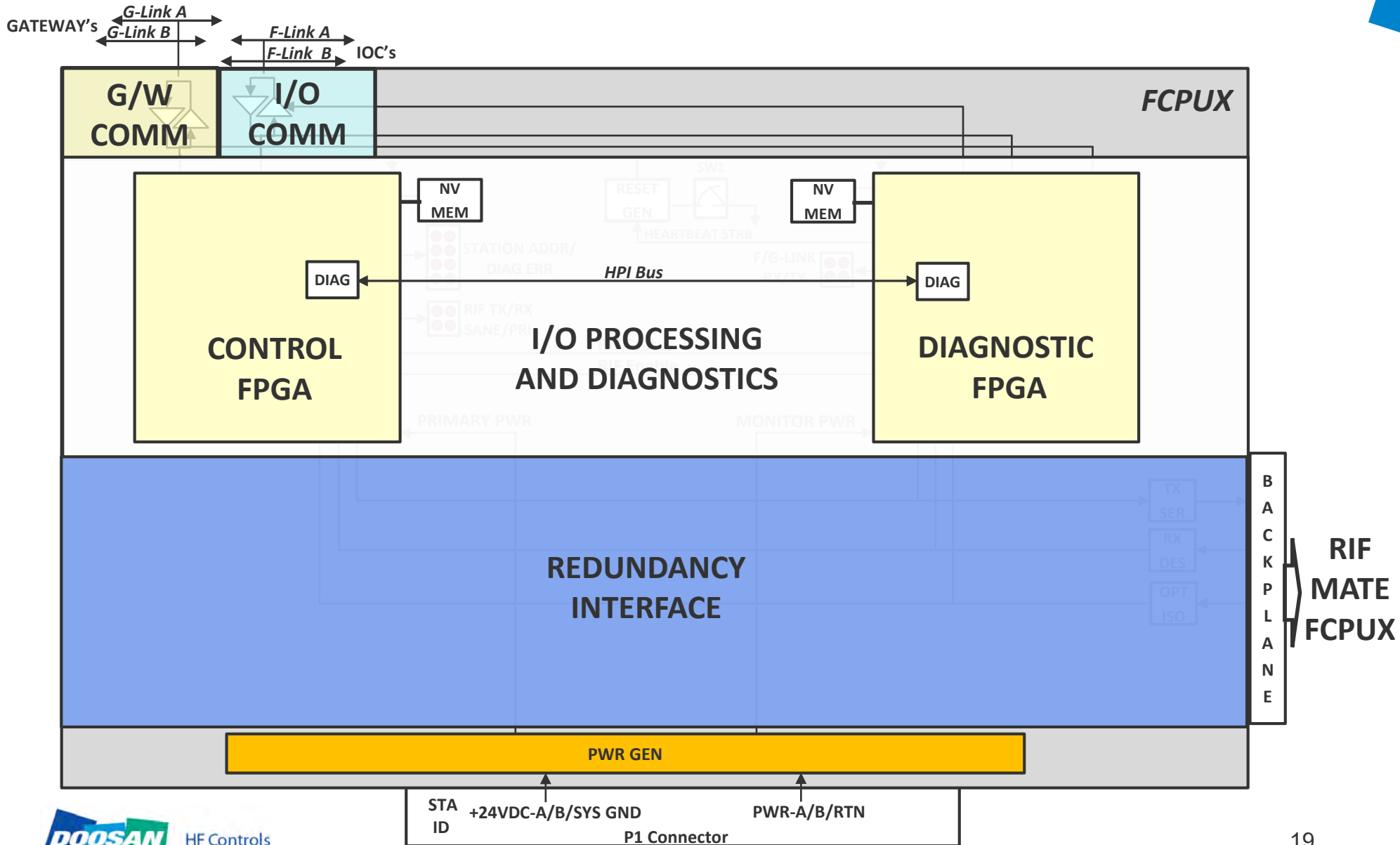
- ❖ FPGA based controller with diagnostics capabilities
- ❖ Intelligent module diagnostics and self checking capabilities
- ❖ Power on reset circuitry with onboard watchdog timer
- ❖ Redundant power feeds with onboard diode auctioneering
- ❖ Redundant communications interfaces
- ❖ Onboard status LED indications

Functional Description

- ✓ The HFC-FCPUX is a central control unit designed for use in the HFC-FPGA product line.
- ✓ The HFC-FCPUX supports communications with FPGA FPU I/O modules via F-Link, Gateway Controller via G-Link, and its redundant controller via the RIF.
- ✓ The two FPGAs on the HFC-FCPU is partitioned into Control FPGA and Diagnostic FPGA. They are intended to work in tandem, processing the same input to compare and validate output data.
- ✓ The dual FPGA structure is designed to protect final output data from Single Event Upset, and single component failure that may impact safety function.
- ✓ The HFC-FCPU circuit structure includes multiple layers of function safety protection circuitry/logic to enforce the DI/DO channel verification and communication data acquisition/verification.



FCPUX (FPGA CONTROLLER) ARCHITECTURE



HFC-FPGA I&C APPLICATION UTILITY – ONESTEP

- USES SIMILAR METHOD OF ENTRY TO HFC-6000 MICROPROCESSOR SYSTEM

The screenshot displays the HFC-FPGA I&C Application Utility software. The main window shows a complex wiring diagram with various components and connections. A 'Select Icon - HFC' dialog box is open in the foreground, displaying a list of available components such as 'MAN AUTO BLOCK', 'CONTROLLER WITH SETPOINT & PV', 'CALCULATION BLOCK', etc. The background window is an AutoCAD 2000i interface showing the same diagram in a CAD environment.

Select Icon - HFC

Exit Edit Settings

Name: Search: OK Symbol

Descriptor: Macro

Symbol Settings:	Angle:	Scale:	Mirror:	Maintain Device IDs As Created
	0	1.0000	Off	-
Macro Settings:	0	1.0000	-	No

Analog logic [basic]
 Digital logic
 J212-DE J11-11
 Kepco_I/O_cards
 Kepco_functional_I/O_cards
 Kepco_logic_templates

B 1 BL_1 MAN AUTO BLOCK	AVG BL_7 AVERAGING BLOCK
5 P 0-100 % PID BL_2 CONTROLLER WITH SETPOINT & PV	FCI BL_8 CHARACTERIZING BLOCK
4 2 1 3 5 CAL BL_3 CALCULATION BLOCK	D 1 BL_9 DIVIDE BLOCK
EXT BL_3 EXTENDED BLOCK MEMORY STORAGE	S BL_10 HIGH SELECT BLOCK
A-20 MA AIC BL_4 ANALOG INPUT BLOCK	L BL_11 LOW SELECT BLOCK
0-100 % AOP BL_5 ANALOG OUTPUT BLOCK	LCC BL_12 LEAD LAG BLOCK
DIG BL_13 DIGITAL HIGH ALARM BLOCK	
DIA BL_14 DIGITAL LOW ALARM BLOCK	

AutoCAD 2000i - NETWORK VERSION - [C:\PROMIS-EX\PROJECT\WORK\3.ECI\3.ECI\1.dwg]

File Edit View Insert Format Draw Modify Manage Tools Reports Help

Device ID
Part Number
Connection Point
Device Type
Symbol Text
PLC Text
Device Type Cross Reference Toggle
Move
Rotate
Text Position
Text Angle
Attribute Settings
Block Settings

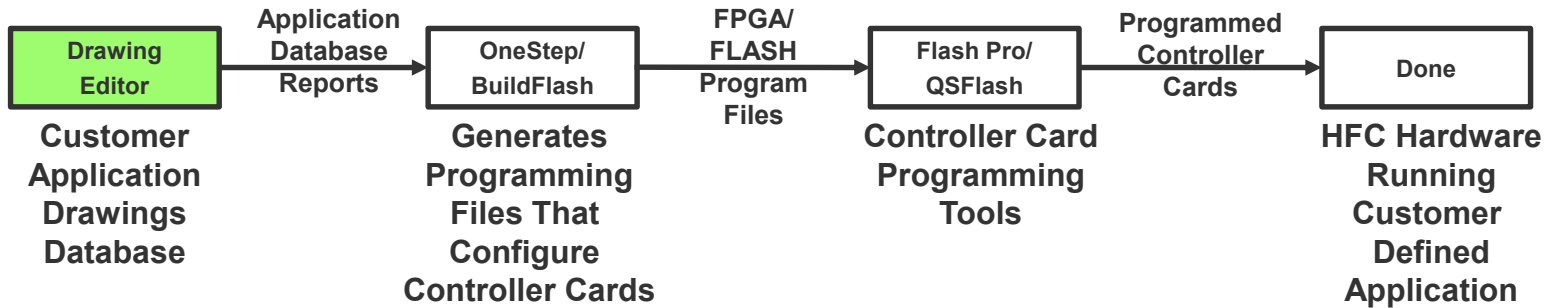
Model Layout

1: (elisa "POWER EDITOR 2")
2: (elisa "POWER EDITOR 2")

0342 Lt. 1. Dn [29.2453, 16.6142, 0.0000] SNAP | GRID | ORTHO | POLAR | OSNAP | OTRACK | LWT | MODEL

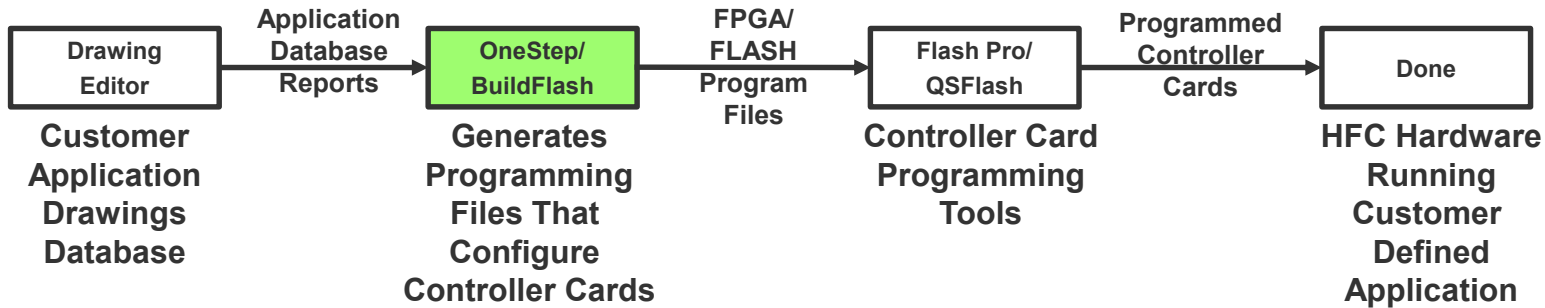
AutoCAD 2000i - NET... Exploring - Stand Users M... onestepRevB - Microsoft 10:04 AM

HFC-FPGA AUTOMATED LOGIC GENERATION



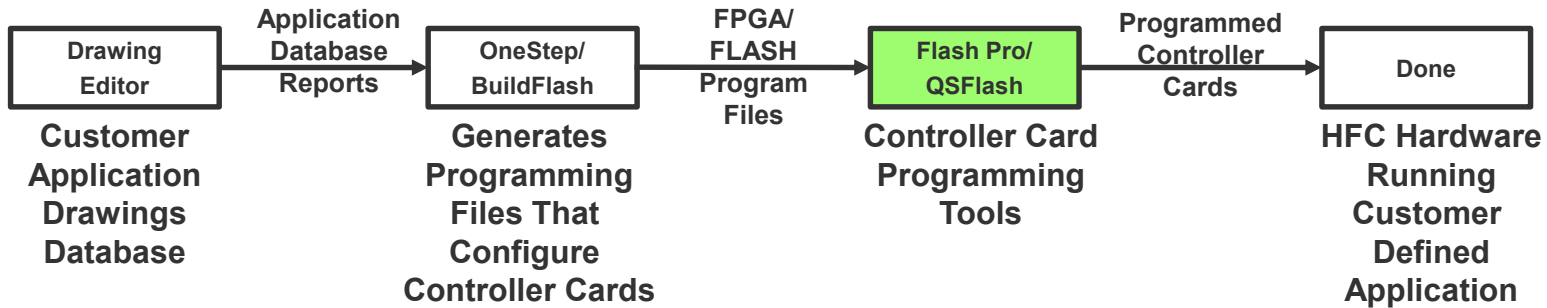
- **APPLICATION IS DEFINED BY THE GENERATION OF A SET OF CAD DRAWINGS**
 - PROMISE CURRENTLY SUPPORTED
 - SCHEMATIC TYPE REPRESENTATION OF THE APPLICATION
 - PROCESSING OF THE DRAWING SET CREATES APPLICATION DATA BASE REPORT
- **DRAWING SET IS PROCESSED BY ONESTEP**
 - ONESTEP IS A NRC QUALIFIED TOOL DEVELOPED BY HFC

HFC-FPGA AUTOMATED LOGIC GENERATION



- **INVOKING ONESTEP GENERATES PROGRAMMING FILES THAT CUSTOMIZE THE HFC-6000 FPGA SYSTEM**
 - PARSES DRAWING DATABASE
 - DETERMINES THE ORDER OF ANALOG PROCESSING (IF REQUIRED)
 - REQUIRED APPLICATION LOGIC RTL
 - ANALOG PROCESSING (CQ4) REQUIREMENTS
 - F-LINK FILTERING
 - MEMORY INITIALIZATION
 - INVOKES LIBERO (MICROSEMI FPGA SOC TOOL) TO GENERATE FPGA PROGRAMMING FILES USING THE FOLLOWING INPUTS
 - PUBLISHED PLATFORM BLOCKS
 - APPLICATION LOGIC RTL
 - BUILD SCRIPTS GENERATE PROGRAMMING FILES FOR THE DIAGNOSTIC AND CONTROL FPGA'S
 - HFC BUILDFLASH TOOL GENERATES BINARY FLASH PROGRAMMING FILE

HFC-FPGA AUTOMATED LOGIC GENERATION



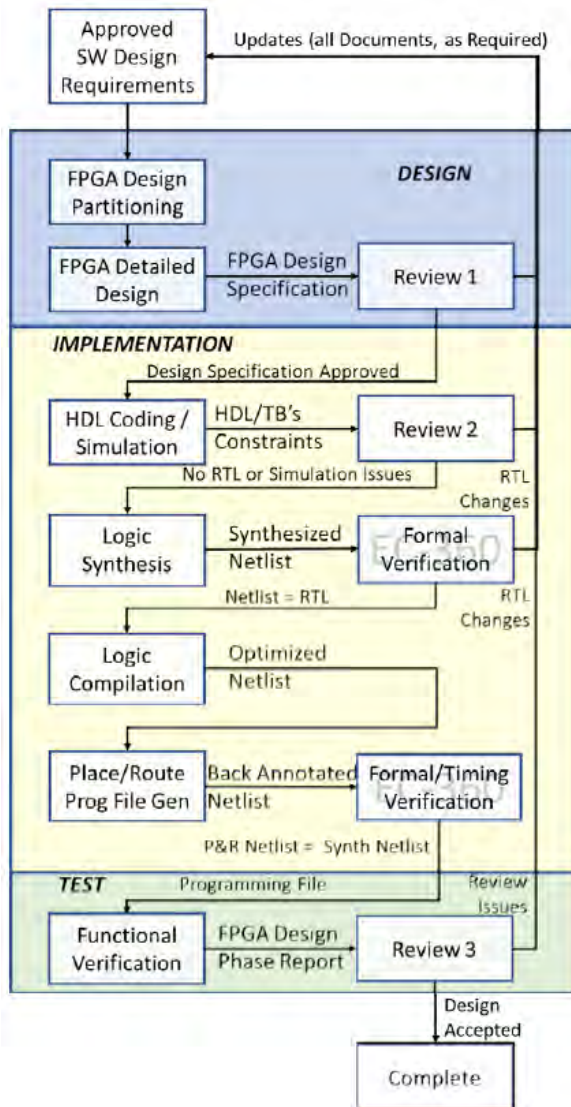
- **FLASH PRO (MICROSEMI TOOL)**

- USES ONESTEP GENERATED FPGA PROGRAMMING FILES TO CONFIGURE THE FCPUX CONTROL AND DIAGNOSTIC FPGA'S

- **QSFLASH**

- HFC UTILITY USED TO PROGRAM CONTROL AND DIAGNOSTIC SPI FLASH WITH A PC USB PORT
 - REQUIRES THE HFC 40134221Q SPI FLASH PROGRAMMER

FPGA DESIGN PROCESS



- ✓ **DESIGN PHASE INPUT**
 - ✓ APPROVED SW REQUIREMENT SPECIFICATION
- ✓ **DESIGN ACTIVITIES**
 - ✓ PARTITIONING AND DETAILED DESIGN
 - ✓ OUTPUT – APPROVED DESIGN SPECIFICATION
- ✓ **IMPLEMENTATION PHASE INPUT**
 - ✓ APPROVED DESIGN SPECIFICATION
- ✓ **IMPLEMENTATION ACTIVITIES**
 - ✓ CODING, SYNTHESIS, PLACE AND ROUTE
 - ✓ FORMAL VERIFICATION – VALIDATE SYNTHESIS, P&R
 - ✓ OUTPUT - VALIDATED P&R NETLIST, PROGRAMMING FILES
- ✓ **TEST PHASE INPUT**
 - ✓ PROGRAMMING FILE GENERATED FROM IMPLEMENTATION
- ✓ **TEST ACTIVITIES**
 - ✓ DEVICE VALIDATION
 - ✓ FUNCTIONAL VERIFICATION

HFC-FPGA PRODUCT SUMMARY

- **HFC-FPGA IS AN EVOLUTION OF THE HFC-6000 PRODUCT THAT REMOVES MICROPROCESSOR CONTROL ELEMENTS**
 - SHARES IMPORTANT AND NECESSARY QUALITIES OF THE HFC-6000 SYSTEM
 - BUILDS ON THIS PLATFORM BY ADDING DETERMINISTIC STATE MACHINE PROCESSING AND REDUNDANCY
 - REPLACE ICL PROTOCOL (MASTER/SLAVE) WITH A TOKEN PASSING PROTOCOL CALLED F-LINK
 - CONTROL FPGA – MAIN CONTROL ELEMENT
 - DIAGNOSTIC FPGA – VERIFIES ACTIVITY AND PROCESSING RESULTS OF THE CONTROL FPGA
 - SHARES HFC-6000 TOOLS FOR DEVELOPING APPLICATIONS
 - IMPLEMENTS REDUNDANCY OVER A SEPARATE REDUNDANCY INTERFACE
- **TWO SYSTEM CONFIGURATION OPTIONS – DISTRIBUTED AND CENTRALIZED**
 - DISTRIBUTED, I/O FPU RUN A PORTION OF THE APPLICATION
 - CENTRALIZED, FCPUX RUNS APPLICATION WITH INPUT AND OUTPUT PROVIDED BY THE FPU
- **CONTROL APPLICATION STORAGE**
 - FPGA CONFIGURATION AND REDUNDANT NON-VOLATILE MEMORY ELEMENTS
 - FPGA'S VALIDATE APPLICATION AT POWERUP USING INTRA-FPGA BUS

THANK
YOU