The Application of FPGA-based FitRel Platform in Nuclear Power Plant Diverse Actuation System

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1 Introduction

2 R&D of FPGA-based FitRel Platform

3 Application in ACPR1000 Project

4 Conclusion
1.1 Introduction - CTEC

We are

The 1st enterprise having developed its own safety DCS product in China

The 1st enterprise from China being able to provide an integrated DCS solution to nuclear power customers

The 1st National Energy R&D Center for NPP Digital I&C System in the industry

Over 200 successful cases in nuclear power industry

China Techenergy Co., Ltd.
A joint venture co-funded by China Nuclear Power Engineering Co., Ltd. (CNPEC, the controlling shareholder) and Beijing Hollysys Co., Ltd. (HOLLYSYS), provides full-life-cycle and end-to-end digital instrument and control (I&C) solutions to nuclear power customers.
1.1 Introduction - CTEC

A platform developed by CTEC with its own intellectual property for the safety applications, such as RPS (reactor protection system), ESFAS (engineered safety features actuation system) and PAMS (post accident monitoring system), as well as the safety-related instrumentation and control systems.

A general platform developed based on the FPGA (Field Programmable Gate Array) technology for the diversity of safety systems. It is applicable to nuclear power plants of various technologies.

A matured platform for the non-safety DCS which has already been used for many nuclear power plants under construction in China.

A platform designed for various specific NPP DCS, such as KDO, KME, EPP, LSS, TRA, and KSN, which is mainly featured in fast and high-accuracy data acquisition and wave record.

A self-developed nuclear emergency information management system platform, which can be customized to the application in nuclear power plants, power-generation groups, and provincial and national levels.
1.1 Introduction - CTEC

More than 300 I&C Projects
1.2 Introduction - FitRel Platform Positioning

FitRel

General FPGA-based NPP I&C

- DAS (Diversity Actuation System) for RPS as Non-safety.
- Achieving protection function with another safety I&C protection system.
- Protection system for specific application.
1.3 Introduction - FitRel Platform Roadmap

National 863 Program (sub-project)
The Research of Diversity technology of I&C in NPP

Development of diversity I&C device in NPP

Development of FitRel-1000 platform released

Hongyanhe Unit 5,6

Tianwan Unit 5,6

Yangjiang Unit 5,6

Fangchenggang Unit 3,4

2012 2013 2014 2015 2016 2017
1.4 Introduction- Standard

- **Logic design:** IEC-62138 category B
  IEC-62566, NUREG/CR7006
- Logic V&V: IEEE1012 Class 3
- Hardware design: IEC-60987, IEC 60780
- Environment Test:
  IEC 60068-2 (Class 3)
- Seismic Test:
  Seismic category 1, GB/T 13625
- Electromagnetic Compatibility:
  IEC 62003 (Class 3)
2.1 Architecture Design

- Take the advantage of **parallel processing** of FPGA, improving the speed and efficiency of arithmetic operation;
- Retain the advantage of the modern centralized DCS, and the configuration, management and scheduling of the entire system are performed by the main process unit, therefore, the system still has a strong ease of use;
- **Generic FPGA (GFPGA) and Application FPGA (AFPGA);**
- 4 AFPGAs support complex algorithm processing.
## 2.2 Functional Safety Design

### SIL3

<table>
<thead>
<tr>
<th>Component</th>
<th>Function block</th>
<th>Diagnose measure</th>
<th>DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>Clock</td>
<td>Independent time base and time window</td>
<td>H 99%</td>
</tr>
<tr>
<td>Data integrity</td>
<td>CRC32/64</td>
<td>H 99%</td>
<td></td>
</tr>
<tr>
<td>Comm interface</td>
<td>Safety protocol</td>
<td>H 99%</td>
<td></td>
</tr>
<tr>
<td>Application logic block</td>
<td>Built-in self test</td>
<td>M 90%</td>
<td></td>
</tr>
<tr>
<td>Clock</td>
<td>Quartz, Oscillator,PLL</td>
<td>WDT of independent time base and time window</td>
<td>H 99%</td>
</tr>
<tr>
<td>Digital input</td>
<td>Redundant input signal compare</td>
<td>M 90%</td>
<td></td>
</tr>
<tr>
<td>Digital output</td>
<td>Read back &amp; dynamic self-test</td>
<td>M 90%</td>
<td></td>
</tr>
<tr>
<td>Analogue input</td>
<td>Dynamic self-test</td>
<td>M 90%</td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>Over-voltage</td>
<td>Voltage monitor and compare</td>
<td>H 99%</td>
</tr>
<tr>
<td></td>
<td>Under-voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Safety communication</td>
<td>Transmission errors;</td>
<td>H 99%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Repetitions;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Deletion;</td>
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<tr>
<td></td>
<td>Insertion;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Re-sequencing;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Corruption;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Delay;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Masquerade.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.3 Hardware and Mechanical Design

- 19 inch standard
- 40U installation space
- Seismic class I

- FPGA-based
- High DC SIL3
- Reliability
- Power
- Clock
- EMC
- Cooling
- Derate
2.4 HPD Design

**Design Phase**

- **Synchronous design**
  - It makes the design simpler and more deterministic, and it facilitates verification and testing;

- **Modular design**
  - Use of smaller, simpler modules as opposed to one large;

- **Segregating the primary functions**
  - Maintenance function like transmitting, diagnose information;

- **Avoid using complex native blocks**
  - FitRel platform supplies sufficient application algorithm blocks without any the third party IP, even the basic blocks like addition, multiplication, divisions, etc.

**Traditional “V cycle” model**
2.4 HPD Design

Implementation phase
- Synthesis and place and route
- Static Timing Analysis (STA)

Verification and validation phase
- RTL simulation
- divide et impera’ (divide and conquer) principle
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3.1 Application projects

2015年 Unit5&6 Yangjiang NPP  DAS
2015年 Unit5&6 Hongyanhe NPP  DAS
2016年 Unit5&6 Tianwan NPP  DAS & ECP
2016年 Unit5&6 Fangchenggang DAS (Hualong One)
3.1 DAS Architecture

DAS function

• Providing diversified automatic signals to actuate reactor trip and the chosen engineering safety features
• Providing diversified manual reactor trip and actuation of the engineering safety features
• Providing diversified independent indicators for chosen power plant parameters
3.1 DAS Architecture

LEVEL2:
- Server + VDU
- Hardware manual
- Display instrument
- Indicator
- Maintenance tool

LEVEL1:
- 2 auto actuation logic cabinets
- 2 manual actuation logic cabinets

2002
### 3.2 DAS Performance

#### Technical Index

<table>
<thead>
<tr>
<th>Index</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA memory</td>
<td>≤70%</td>
</tr>
<tr>
<td>Load of network</td>
<td>≤40%</td>
</tr>
<tr>
<td>Analog input signal</td>
<td>± 0.1%</td>
</tr>
<tr>
<td>Analog output signal</td>
<td>± 0.1%</td>
</tr>
<tr>
<td>Rejection rate</td>
<td>0.01/instruction</td>
</tr>
<tr>
<td>Spurious rate</td>
<td>0.1 time per year</td>
</tr>
<tr>
<td>Availability</td>
<td>&gt;99.99%</td>
</tr>
<tr>
<td>Response time</td>
<td>150ms</td>
</tr>
</tbody>
</table>

#### DAS and RPS Diversity Analysis Result

<table>
<thead>
<tr>
<th>Dimension</th>
<th>DCE WT</th>
<th>INH</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design</td>
<td>1</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Equipment Manufacture</td>
<td>0.25</td>
<td>0.075</td>
<td>0.3</td>
</tr>
<tr>
<td>Logic Processing Equipment</td>
<td>0.64</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Functional</td>
<td>0.6</td>
<td>0.6</td>
<td>1</td>
</tr>
<tr>
<td>Life-Cycle</td>
<td>0.683</td>
<td>0.4098</td>
<td>0.6</td>
</tr>
<tr>
<td>Signal</td>
<td>0.867</td>
<td>0.72</td>
<td>0.83333</td>
</tr>
<tr>
<td>Logic</td>
<td>0.733</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Score = 1.287184908 > 1.0**
3.3 Difficulties

Usability problem
- Graphical algorithm configuration tools;
- Algorithm download based on Ethernet technology.

Diversity problems
- It is recognized by most of the countries according to NUREG/CR-6303/7007
- Difficult for GDA of UK, Simple Hardware Technology

V&V problems
- Build FitRel simulation platform carried full validation and verification.
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1 Achievement
The first FPGA-based digital I&C platform applied in diversity actuation system in China. The application was a success with 0 defect for initial powering on. Currently, it is close to commercial operation, and none of FPGA-related problems has occurred.

Features of simplicity, reliability and usability, it is highly appreciated and praised by engineering design teams and owners.

2 Problems
Usability Problems
Diversity Problems
V&V Problems

3 Expectation
Broader and more widespread application of FitRel platform. FPGA Technology will be much more acceptable.
Thank You!