


$$E = mc^2$$

Verification and Validation of FPGA Based Logic Controller

Dec. 6th , 2017

Jang Yeol Kim



한국원자력연구원
Korea Atomic Energy Research Institute

- Table of Contents -

- Overview
 - ❖ Background : Initiative
- QA/SCM
- SA/COTS
- V&V of SRS, SDS and Imp
- Independent Testing(CT, IT and ST)
- Lic. Compliance Check
- Conclusion

Background



○ Needed for 100% Coverage Test for Safety-critical Software

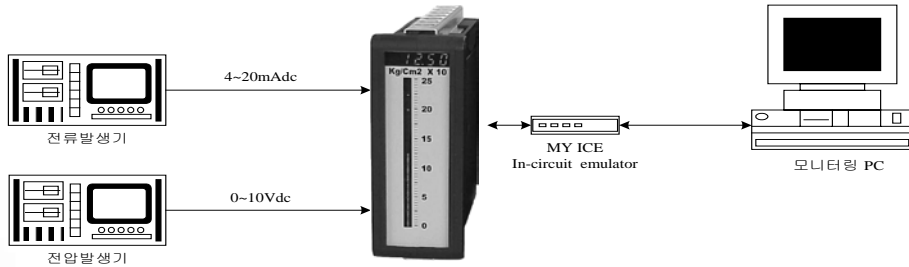
○ Manual Test

– Not Cost Effective

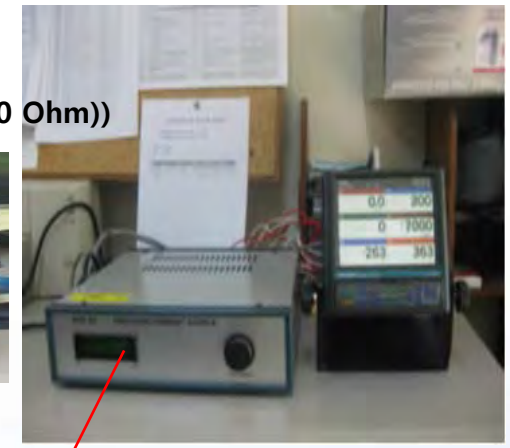
– Too much longer time

○ Needed Exhaustive Testing : Full PATH Testing if possible

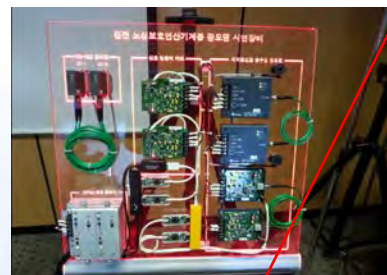
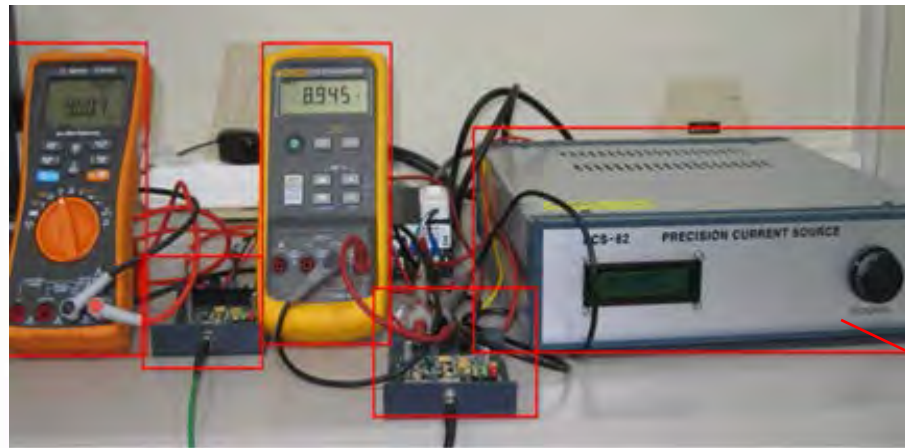
Test Experience : Small Digital Devices



- STEP(2~64) vs DT(01~99)
- 2ms/STEP
- PUSH/Rotation
- Max/Min
- [Voltage : 0.1ms]
- [Current : 1.0000V~5.00V (250 Ohm)]

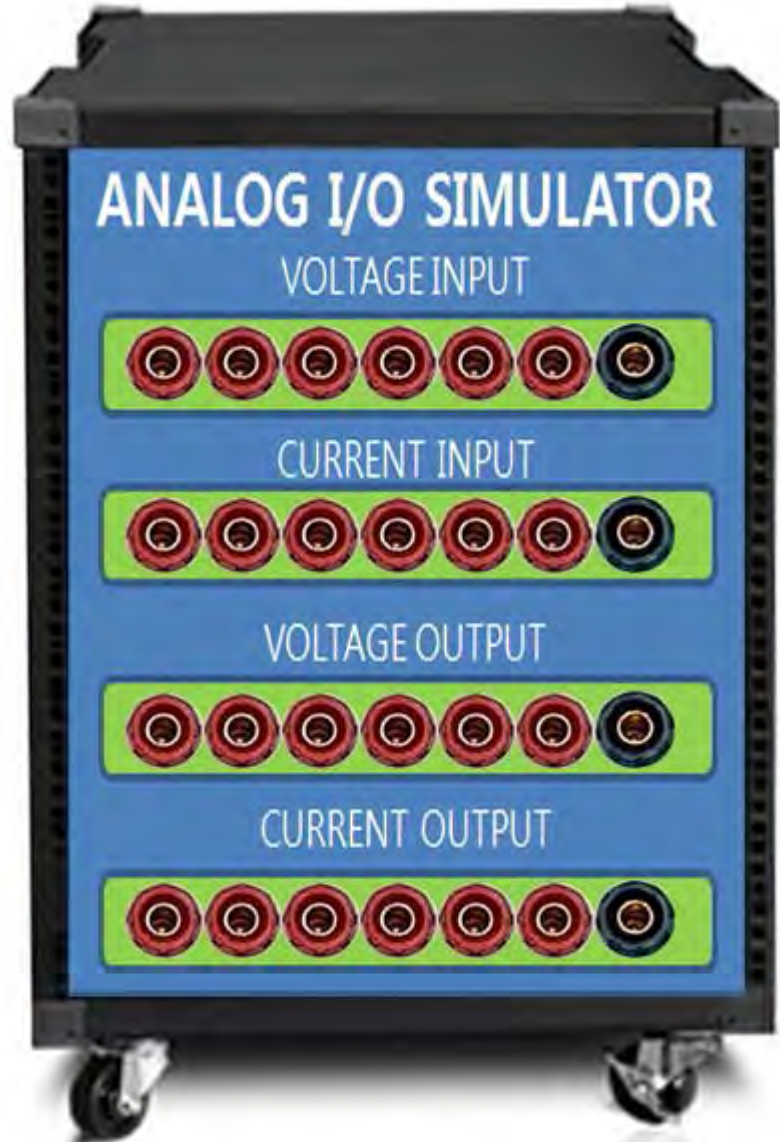


Current : 6CH, Voltage : 2CH



(Automatic Signal Generator)

Manufacturing for Stimulator



ANALOG I/O SIMULATOR SYSTEM

INPUT CHANNEL CONFIG. OUTPUT CHANNEL CONFIG. START SIMULATION STOP SIMULATION

VOLTAGE OUTPUT CONFIG CURRENT OUTPUT CONFIG

VOLTAGE OUTPUT CHANNELS

SET CH No.: CH 0

AUTO LIST MANUAL LIST

START VOLT(V): 0

STOP VOLT(V): 10

VOLT STEP(V): 1

0V 1V 2V 3V 4V 5V 6V

SET APPLY

VOLTAGE CHANNELS CONFIG STATUS

CH No.	START VOLT(V)	STOP VOLT(V)	VOLT STEP(V)	STEP TYPE
CH 0	0	10	1	AUTO

DELETE RESET

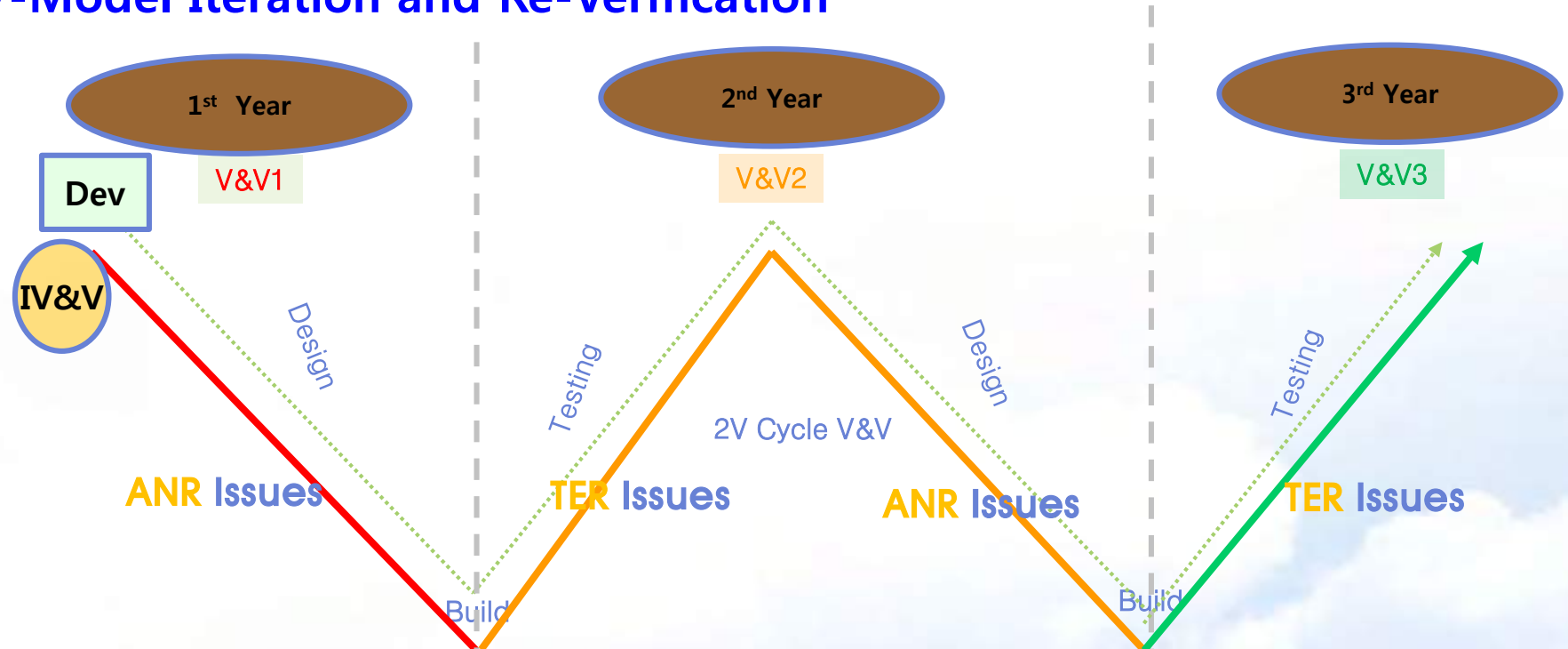
A green arrow points from the software interface to the physical hardware unit.



V&V Schedule (V+V=W Model)

Design : ANR, Testing : TER

V-Model Iteration and Re-Verification



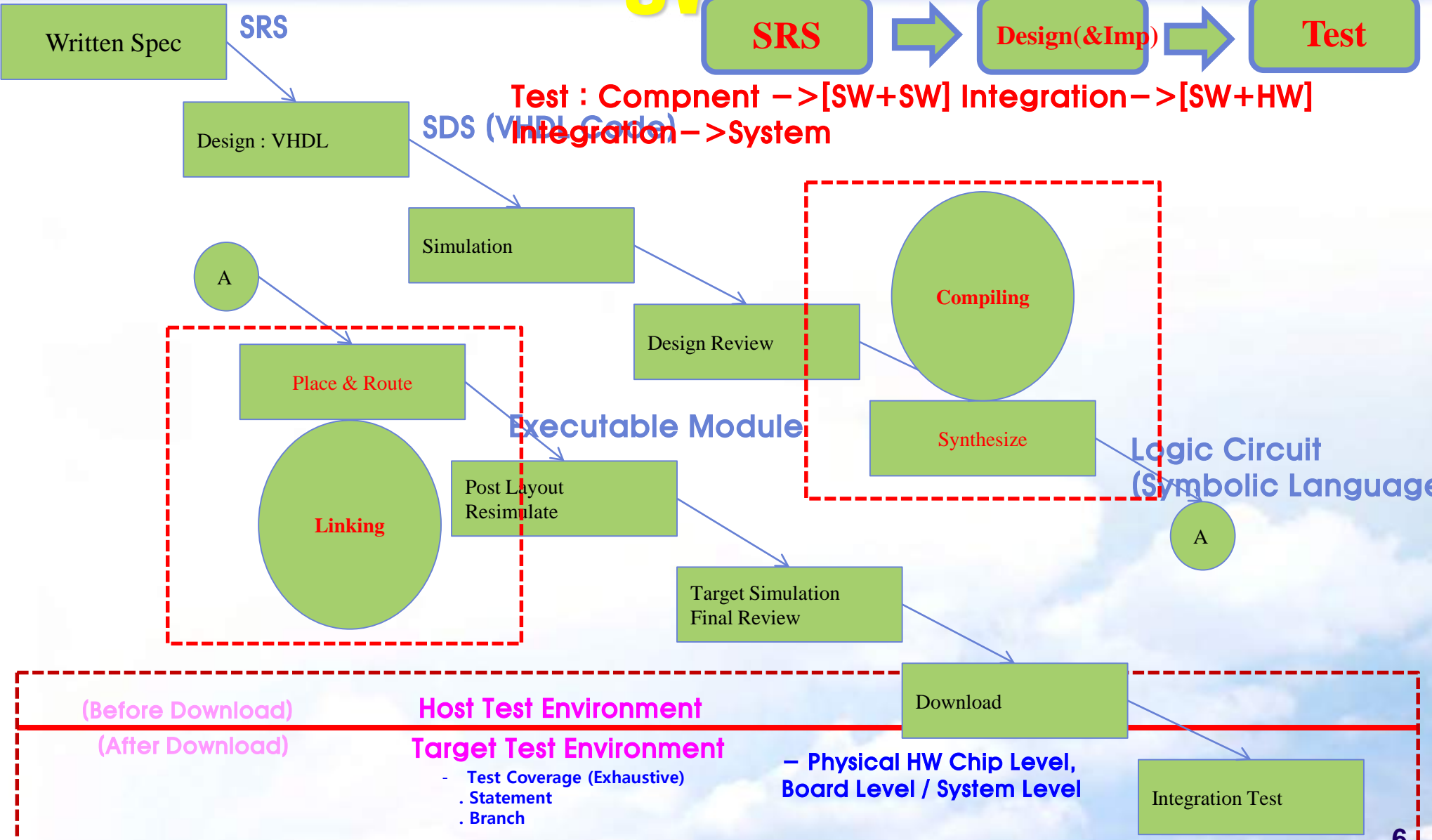
CTR/ITR, STR : Reporting for Dev.
Prj : Anomaly Report (ANR), Test Exception Report (TER)
(Test Case Generation/SW-SW, SW-HW, System, Target . Error Injection, Load Balancing / Burning Test ->
Confirmation of Independent Verifier

Completion of FLC V&V

What is Difference about Traditional SWIC



Test : Component -> [SW+SW] Integration -> [SW+HW]
 Integration -> System



V&V Target : FPGA-based Controller

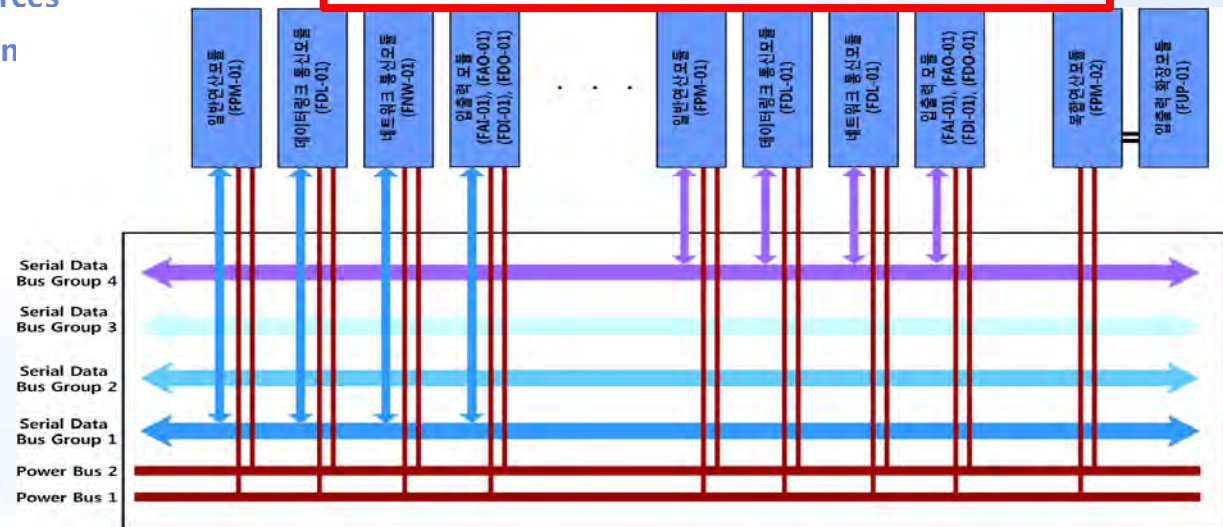
Independent Multi-operation Processing

- Maximum : quadruple operation can be processed.
- Four groups of serial bus applied

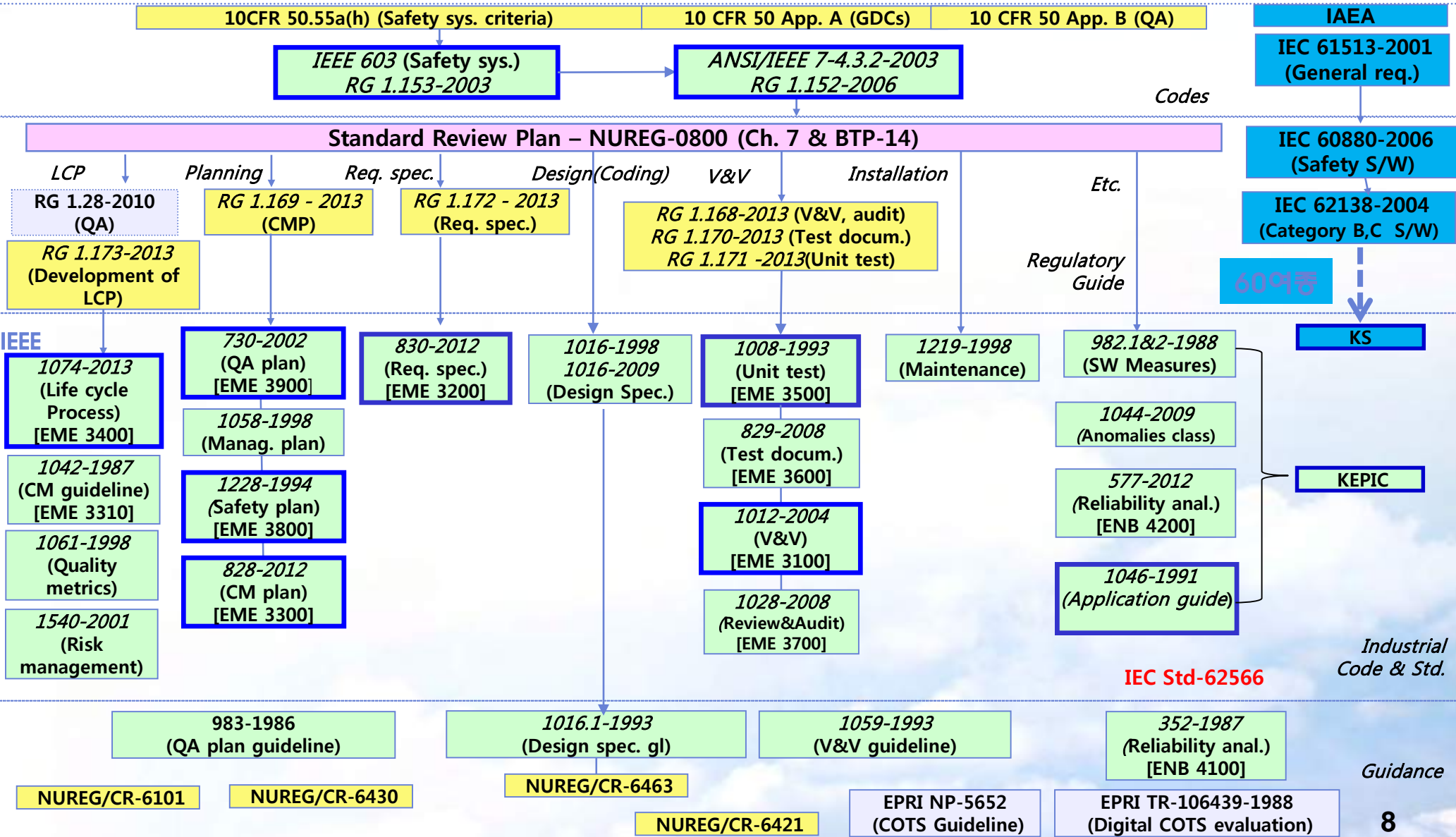


Sub Rack

- Size : 19Inch 6U, 21 slot
- Fan less heat dissipation structure (natural air-cooled type)
- Two independent external power sources
- Front : Front Insertion/Removal System
- Rear : I/O terminal Connector



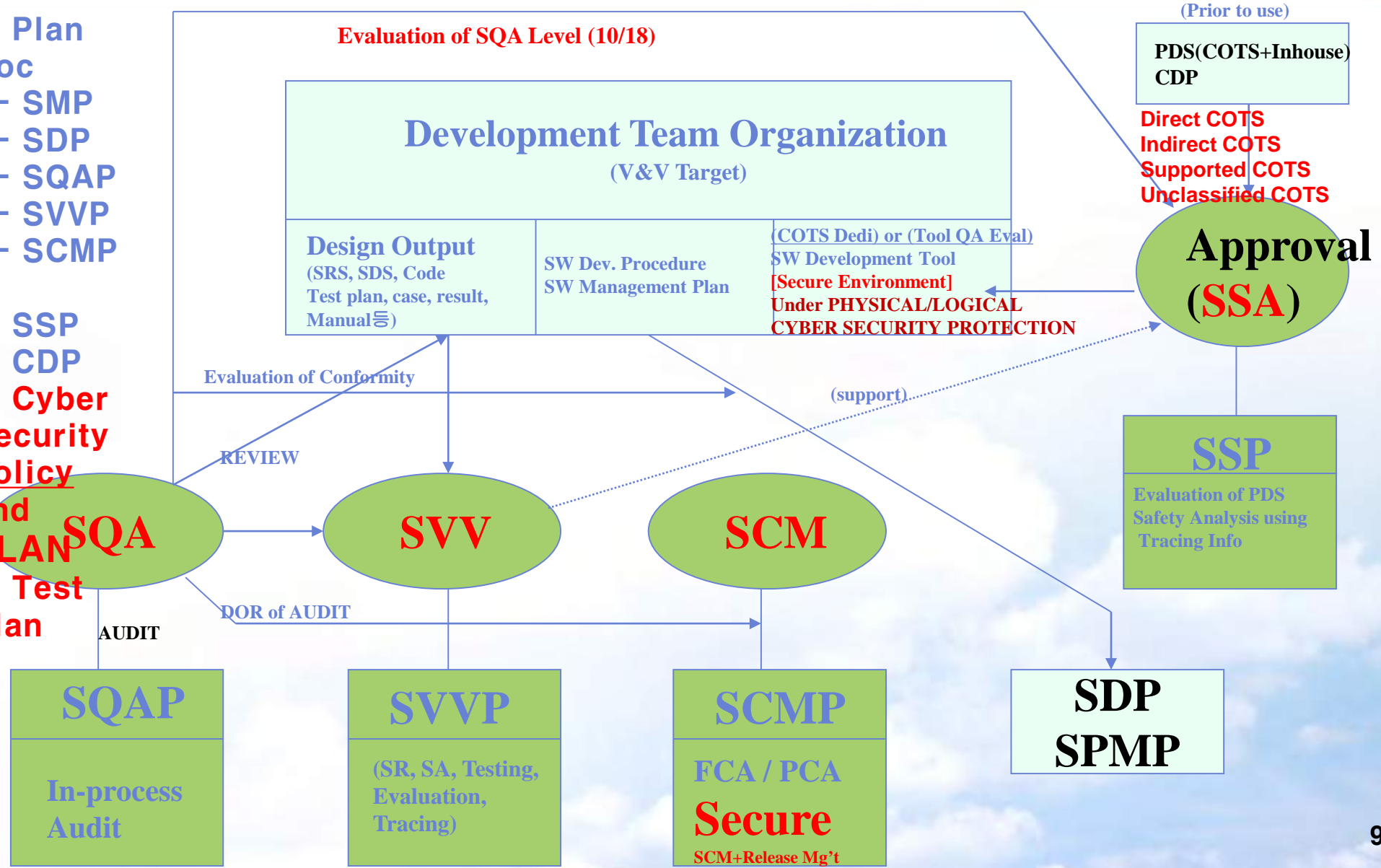
Licensing Requirement



NUREG 0800/BTP-14 : Software Qualification

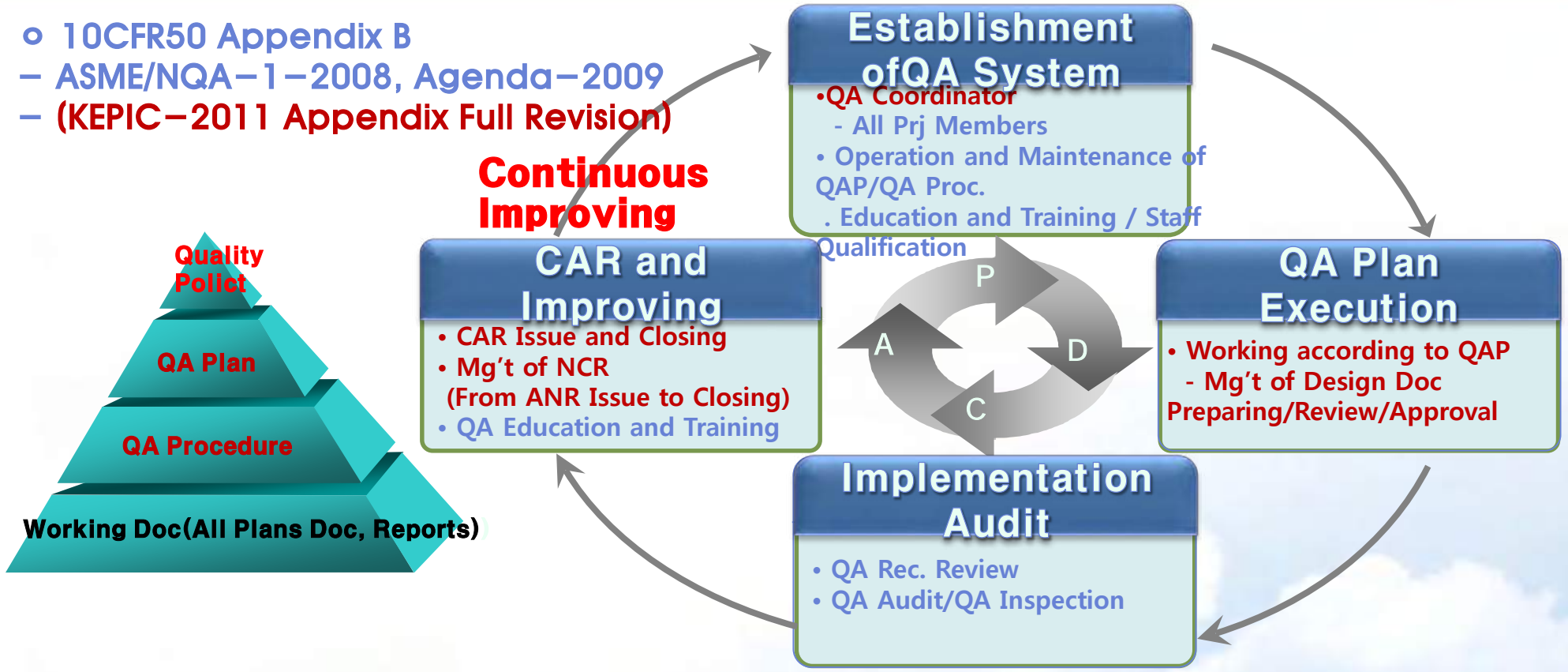
1. Plan Doc
 - SMP
 - SDP
 - SQAP
 - SVVP
 - SCMP

2. SSP
3. CDP
4. **Cyber Security Policy and PLAN**
5. Test Plan



Quality Assurance Activity

- o 10CFR50 Appendix B
- ASME/NQA-1-2008, Agenda-2009
- (KEPIC-2011 Appendix Full Revision)



- Safety and Reliability against CCF
- Licensing Suitability

From ANR/TER issues Opening to Closing

Overall Status Record

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
01

ANR List

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
01

Distribution List

발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
...

The example of baseline list

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
01

TER List

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
111

Items Classification for SWLC

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
01

순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
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순번	항목명	발주처	발주일자	계약일자	계약금액	잔액	잔액비율	잔액상태	잔액일	잔액종류	잔액비율	잔액상태	잔액일	잔액종류
01

Quality Evaluation of COTS SW

COTS SW Dedication 대상 (by NP-5652/TR-106439 + KINS/RG-17.12)

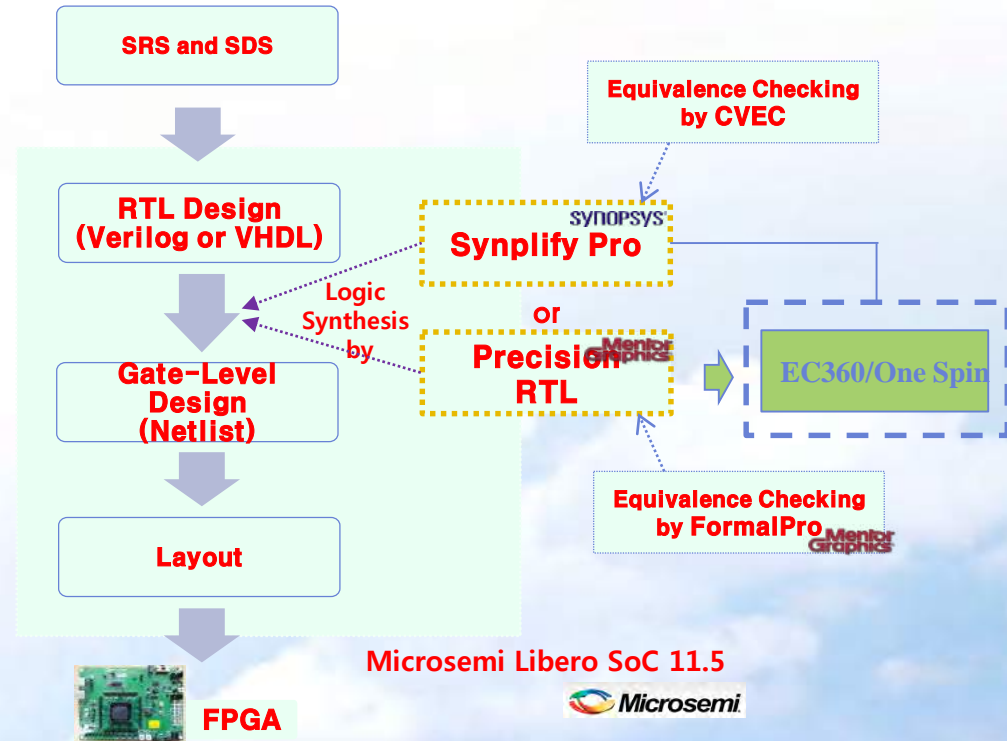
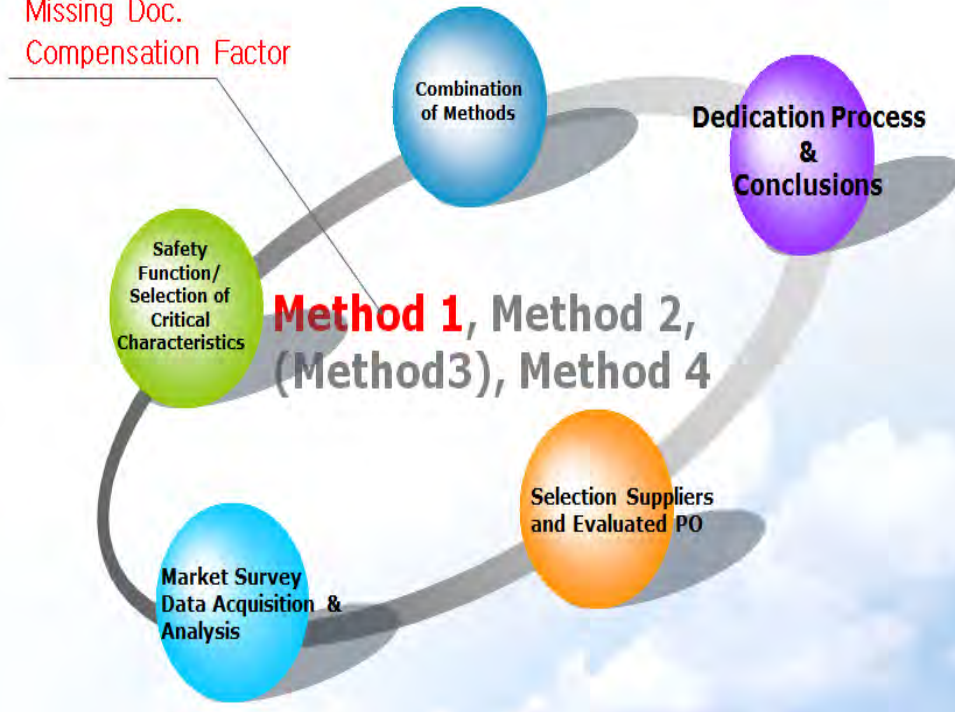
- ❖ Direct SW
- ❖ Indirect SW : Ex) Compiler, Environment Toolset
 - NUREG/CR-6421 : Too Strict
 - EPRI-NP-5652 : HW
 - EPRI-TR-106439 : HW+SW

O Methods

- Special Purpose Testing : Method 1
- Commercial Grade Survey : Method 2
 - . Product Development Record
- Source Verification : Method 3
- Operating Experience Data : Method 4
 - . Correctness
 - . Performance
 - . Software Qualities

In case of COTS Software : Applicable to Method 2 & Method 4

Missing Doc.
Compensation Factor



Safety Analysis of FLC $E=mc^2$

Approaching

- ❖ Safety Analysis Plan
- ❖ Safety Analysis Guideline
- ❖ Deviation : DFLC-N Characteristics
- ❖ Experiences from Past Projects
- ❖ Tracking of V&V Test Results
- ❖ Follow-Up

Deviation
HW Initialization Fail
Memory Initialization Fail
Parameter Setup Missing
Initialization Fail for I/O Updating
Malfunction of FPGA
Stuck at all zeros of ROM/RAM
Memory partition assignment fail
WDT Error

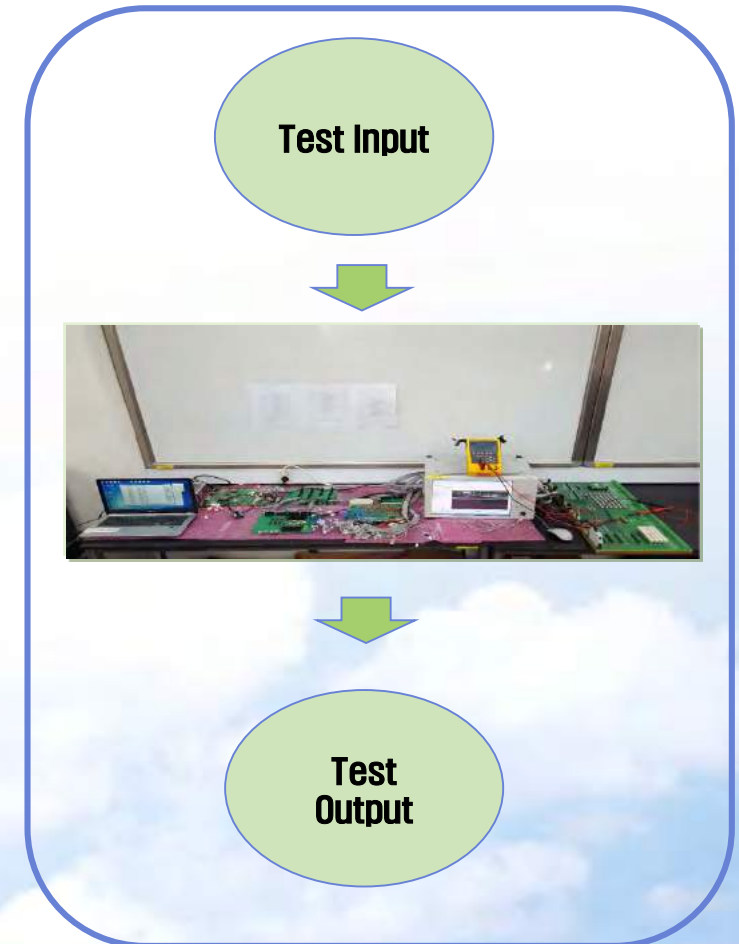


Deviation
Execution Error for Functional Spec
Fail for Reset and Clock Generation Function
Violation of Trigger Condition for Reset and Clock Generation
Termination Violation of Reset and Clock Generation
Fail for Operating Voltage Monitoring
Violation of Trigger Condition for Operating Voltage Monitoring
Termination Violation of for Operating Voltage Monitoring
Fail of Memory Setup and Diagnostics
Violation of Trigger Condition for Memory Setup and Diagnostics
Termination Violation of Memory Setup and Diagnostics
Fail of Inter-Module Data Interface
Violation of Trigger Condition for Inter-Module Data Interface
Termination Violation of for Inter-Module Data Interface
Fail of Data Diagnostics
Violation of Trigger Condition for Data Diagnostics
Violation of Termination Condition for Data Diagnostics

Safety Analysis of FLC

- Safety Analysis and Safety Test based on Recommended Deviation

Deviation	Recommendatiopn
Execution Error for Functional Spec	Confirmation with V&V of Testing Phase
Fail for Operating Voltage Monitoring	“
Violation of Trigger Condition for Operating Voltage Monitoring	“
Termination Violation of for Operating Voltage Monitoring	“
Fail of Memory Setup and Diagnostics	“
Violation of Trigger Condition for Memory Setup and Diagnostics	“
Termination Violation of Memory Setup and Diagnostics	“
Fail of Inter-Module Data Interface	“
Violation of Trigger Condition for Inter-Module Data Interface	“
Violation of Trigger Condition for Inter-Module Data Interface	“
Fail of Data Diagnostics	“
Violation of Trigger Condition for Data Diagnostics	“
Violation of Termination Condition for Data Diagnostics	“



SRS/SDS V&V Report[1]

1. V&V Method and Criteria

- V&V Activities for SRS
 - IEEE Std 1012 + IEC 62566
 - NUREG 0800 Chapter 7/BTP-14
 - Functional and Process Characteristics

Relationship of IEC 62566 and IEEE 1012

IEC 62566	Phase	IEEE Std 1012-2004	Comments
6.6.1	SRS	- Traceability - SRS Evaluation : Correctness, Completeness, Accuracy, Testability - Interface Analysis : Correctness, Consistency	
6.6.2		- Traceability - SRS Evaluation - Interface Analysis	
6.6.3		- SRS Evaluation : Consistency, Completeness, - Interface Analysis : Consistency, Completeness	
6.6.4		- IEEE Std 1012 Appendix C V&V Independence	Technical, Manageable
9.4.1 a)	SDS	- Traceability - Design Evaluation : Completeness, Consistency - Interface Analysis : Completeness, Consistency	
9.4.1 b)		- Design Evaluation : Readability, Testability - Interface Analysis : Testability	
9.4.1 c)		- Traceability - Design Evaluation : Correctness, Consistency, Completeness - Interface Analysis : Correctness, Consistency, Completeness	

SRS/SDS V&V Report [2]

2. SRS V&V Report Revision Report

- The Results of SRS V&V
 - SRS V&V보고서 Rev.0 : Several ANR Issues
 - SRS V&V보고서 Rev.1 : Additional ANR Issues
 - Finally Closing for ANR

The Example of Progress Status on SRS V&V Report

Design Document		V&V Report	
Doc. Number	REVISION	Doc. Number	REVISION
NTIP-FLC-SRS201	Rev.02	NTIP-FLC-RVR501	Rev.01
NTIP-FLC-SRS202	Rev.02	NTIP-FLC-RVR502	Rev.01
NTIP-FLC-SRS203	Rev.02	NTIP-FLC-RVR503	Rev.01
NTIP-FLC-SRS204	Rev.02	NTIP-FLC-RVR504	Rev.01
NTIP-FLC-SRS205	Rev.02	NTIP-FLC-RVR505	Rev.01
NTIP-FLC-SRS206	Rev.02	NTIP-FLC-RVR506	Rev.01
NTIP-FLC-SRS207	Rev.02	NTIP-FLC-RVR507	Rev.01
NTIP-FLC-SRS208	Rev.01	NTIP-FLC-RVR508	Rev.01

3. SDS V&V Report Revision Report

- The Result of SDS V&V
 - SDS V&V Report Rev.0 : Several ANR Issues
 - SDS V&V Report Rev.1 : Additional ANR Issues
 - Finally Closing for ANR

The Example of Progress Status on SDS V&V Report

Design Document		V&V Report	
Doc. Number	REVISION	Doc. Number	REVISION
NTIP-FLC-SDS201	Rev.02	NTIP-FLC-DVR501	Rev.01
NTIP-FLC-SDS202	Rev.02	NTIP-FLC-DVR502	Rev.01
NTIP-FLC-SDS203	Rev.02	NTIP-FLC-DVR503	Rev.01
NTIP-FLC-SDS204	Rev.02	NTIP-FLC-DVR504	Rev.01
NTIP-FLC-SDS205	Rev.02	NTIP-FLC-DVR505	Rev.01
NTIP-FLC-SDS206	Rev.02	NTIP-FLC-DVR506	Rev.01
NTIP-FLC-SDS207	Rev.02	NTIP-FLC-DVR507	Rev.01
NTIP-FLC-SDS208	Rev.01	NTIP-FLC-DVR508	Rev.01

Code V&V Report



1. V&V Method and Criteria

• SRS Criteria Compiling

- IEEE Std. 1012 based Quality Attributes Measurement between Source Code and Implementation Specification
- NUREG 0800 Chapter 7/BTP-14 Acceptable Criteria
 - Licensing Suitability.
- NUREG/CR-7006¹⁾ Code Inspection based on Coding Guideline

IEEE Std 1012 Quality Attributes

Traceability Analysis	Source code and source code documentation evaluation	Interface Analysis
Correctness	Correctness	Correctness
Consistency	Consistency	Consistency
Completeness	Completeness	Completeness
	Accuracy	Accuracy
	Readability	Testability
	Testability	

NUREG/CR-7006 Quality Attributes

Quality attributes
Reliability
Robustness
Traceability
Maintainability

2 Code V&V Report Revision Report

- The Result of Code V&V
 - Code V&V Report Rev.0 : Several ANR Issues
 - Except for CPU, GPM and Communication Module
 - Code V&V Report Rev.1 : Additional ANR Issues
 - Finally Closing for ANR

The Example of Progress Status on Code V&V Report

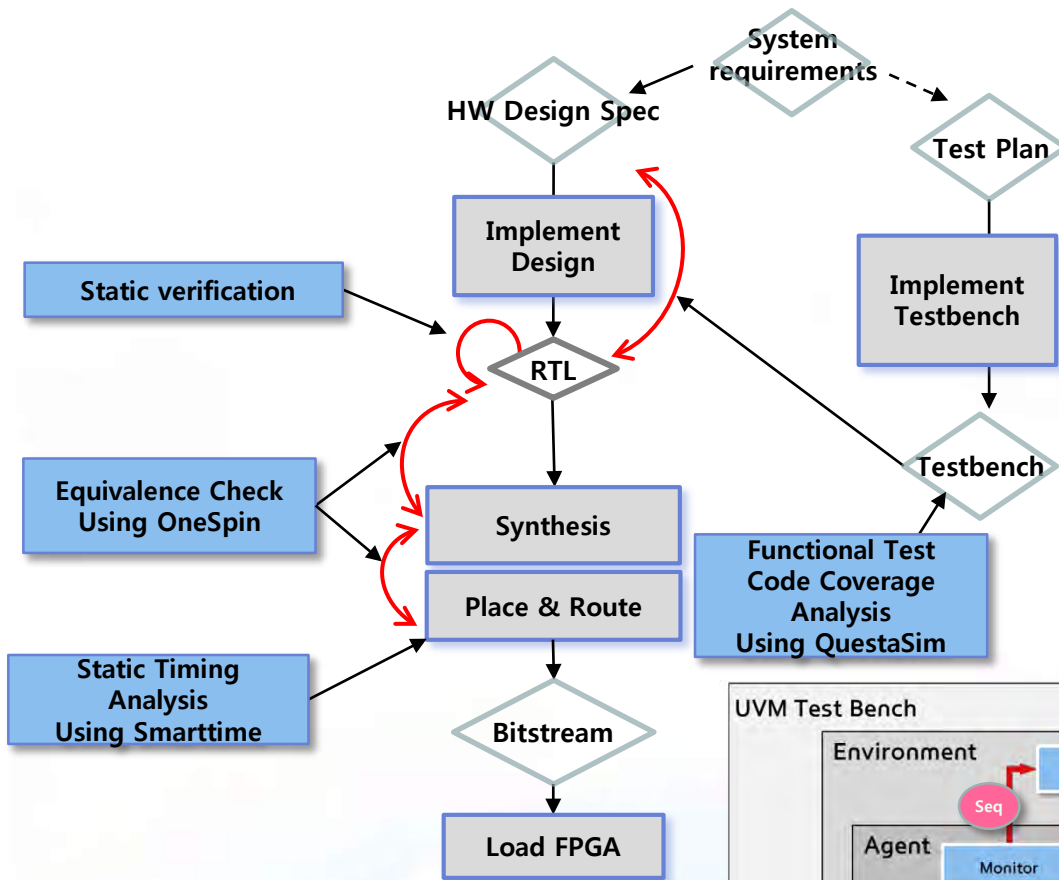
Design Document		Code		V&V Report	
Doc Number	REVISION	Doc Number	REVISION	Doc Number	REVISION
NTP&C-SC001	02	NTP&C-CO001	02	NTP&C-CR001	01
NTP&C-SC002	02	NTP&C-CO002	02	NTP&C-CR002	02
NTP&C-SC003	02	NTP&C-CO003	02	NTP&C-CR003	01
NTP&C-SC004	02	NTP&C-CO004	02	NTP&C-CR004	01
NTP&C-SC005	02	NTP&C-CO005	02	NTP&C-CR005	01
NTP&C-SC006	02	NTP&C-CO006	02	NTP&C-CR006	01
NTP&C-SC007	02	NTP&C-CO007	02	NTP&C-CR007	01
NTP&C-SC008	01	NTP&C-CO008	01	NTP&C-CR008	02

1) FAM-01NUREG CR-7006 : Review Guidelines for Field-Programmable Gate Arrays in Nuclear Power Plant Safety Systems

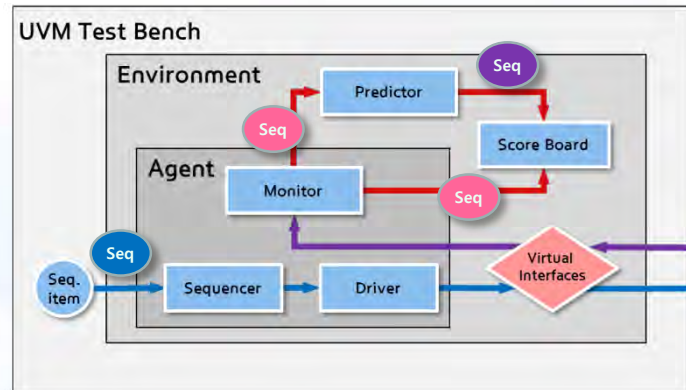
Component Test



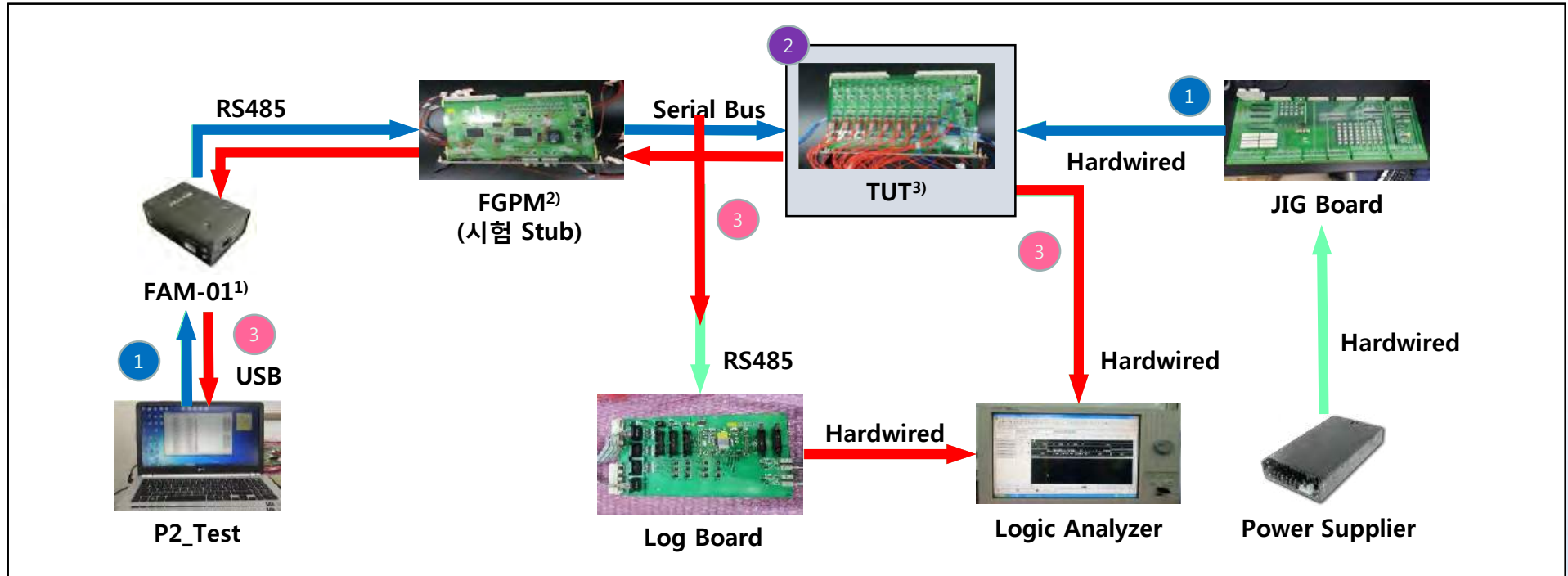
Component Test Procedure



No	Module Name	Signal Name	Expected Output	Actual Output	Pass/Fail	TER No.	Remark
1	clfdi01_top	DGEN	1	1	Pass/c/Fail		
2	clfdi01_top	DIAGSCK	0	0	Pass/c/Fail		
3	clfdi01_top	DIAGLCK	0	0	Pass/c/Fail		
4	clfdi01_top	DIAGSDO	0	0	Pass/c/Fail		
5	clfdi01_top	STEN	0	0	Pass/c/Fail		
6	clfdi01_top	SRXD	1111	1111	Pass/c/Fail		
7	clfdi01_top	LED_RUNP	0	0	Pass/c/Fail		
8	clfdi01_top	LED_RUNN	0	1	Pass/m/Fail	TER-001-NTIP-FLC-CTR505_Rev1	
9	clfdi01_top	LED_FLTP	0	0	Pass/c/Fail		
10	clfdi01_top	LED_FLTN	0	0	Pass/c/Fail		
11	clfdi01_top	LED_STOP	0	0	Pass/c/Fail		
12	clfdi01_top	LED_STON	0	0	Pass/c/Fail		

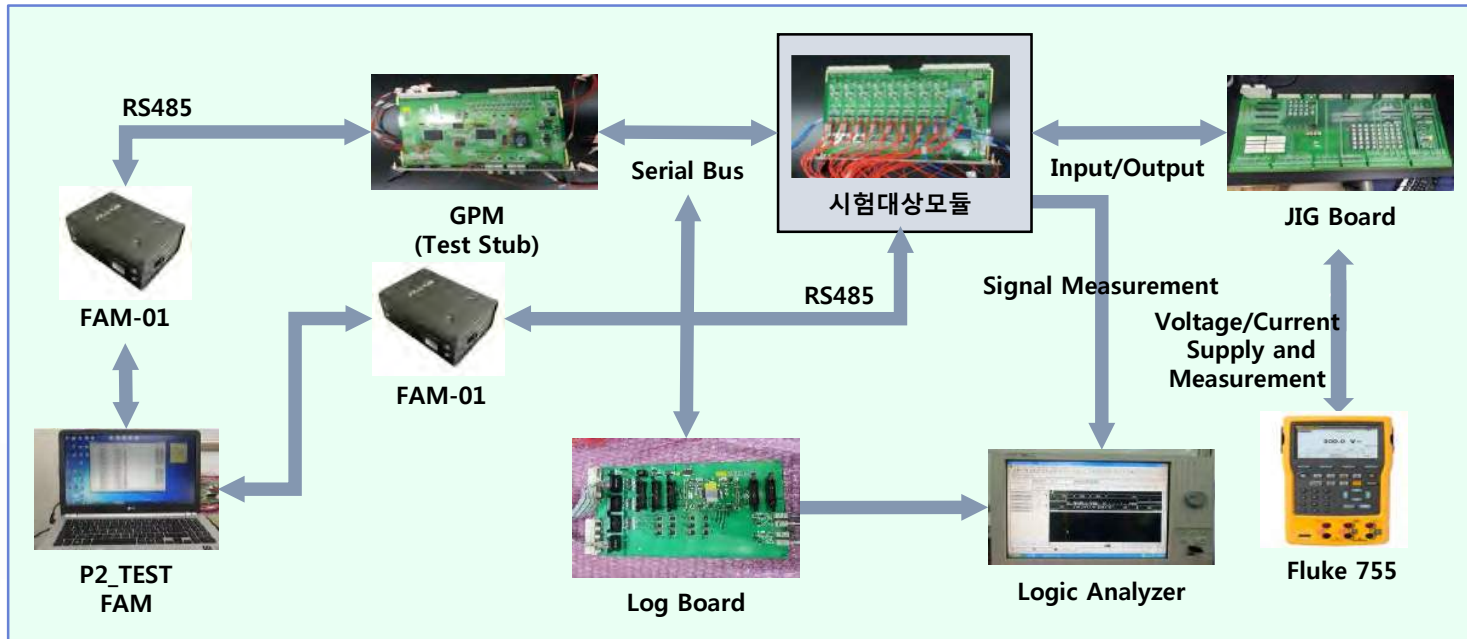


Integration Test[1]



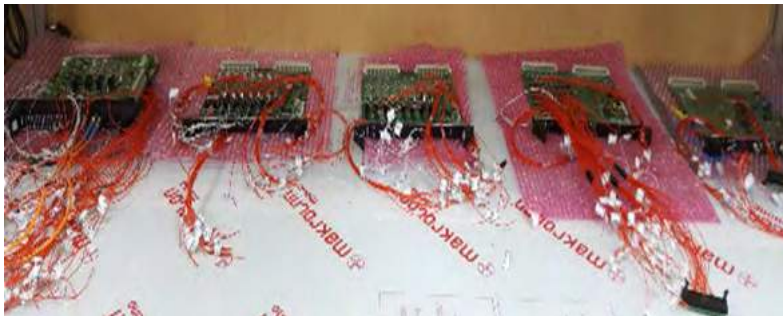
- 1 Test Data Input from P2_Test Software and JIG Board
- 2 Test Execution under Test Conditions with Test Data
- 3 Monitoring through JIG Board and Logic Analyzer

Integration Test[2]



◀ Test Execution Flow

QA Audit DEMO



Real Target Boards ▶ Integration Test Environment



Integration Test[3]

Integration Test

Test Feature: Receiving from Initial Diagnostics Result(Data Frame)

- Check for Receiving from Initial Diagnostics Result(Data Frame) and it's Display status LED.

Test Case: Initial Diagnostics Result Check and LED Check

1) Test Input

No	Name	Value	Description
1	BUS_ID	0	Selection of Bus
2	SET_USE_C H	0xFF	Activation for Channel
3	SET_OP_DIA G	0xFF	Activation for Diagnostics

2) Expected Value

No	Name	Expected Output	Description
1	Slot ID	1f	Slot ID
2	RUN LED	Green	LED Color (Normal Operation)
3	LED_RUNP	0	RUN LED Operation Control (Normal: 0, Process Voltage Error : 1)
4	LED_RUNN	1	

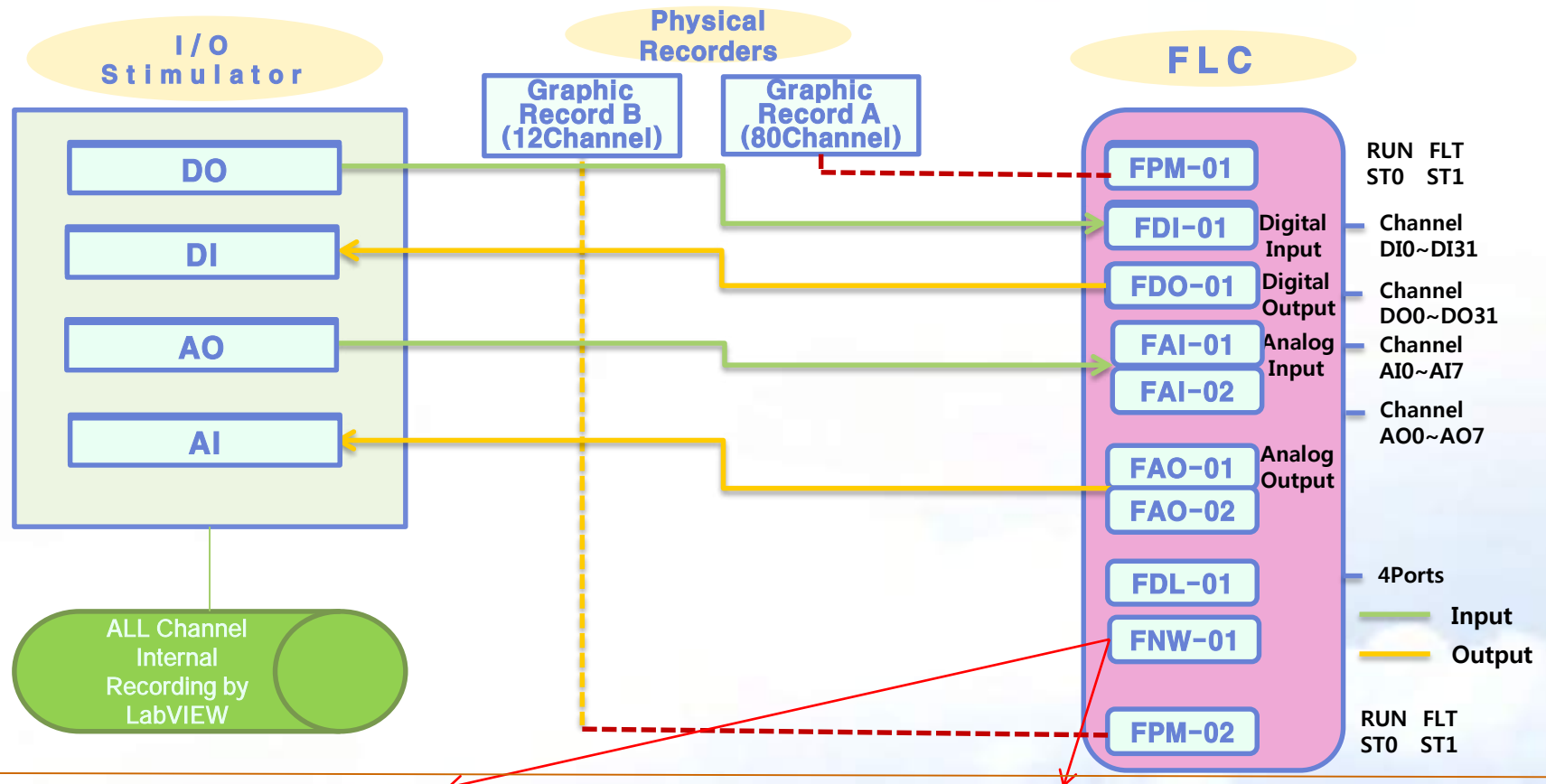
3) Test Output (Logic Analysis)

The logic analyzer shows the following signal levels during the test:

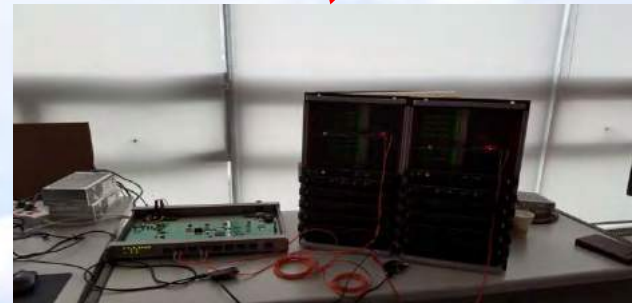
- Slot ID: 1f
- LED_RUNP: 1 (Expected: 0)
- LED_RUNN: 0 (Expected: 1)

Name	Expected Output	Actual Output	Pass/Fail
Slot ID	1f	1f	Pass
LED_RUNP	0	1	Fail
LED_RUNN	1	0	Fail

Independent Testing Platform : Configuration of FPLG based Logic Controller



Switching Test



Functional Test Sending/Receiving

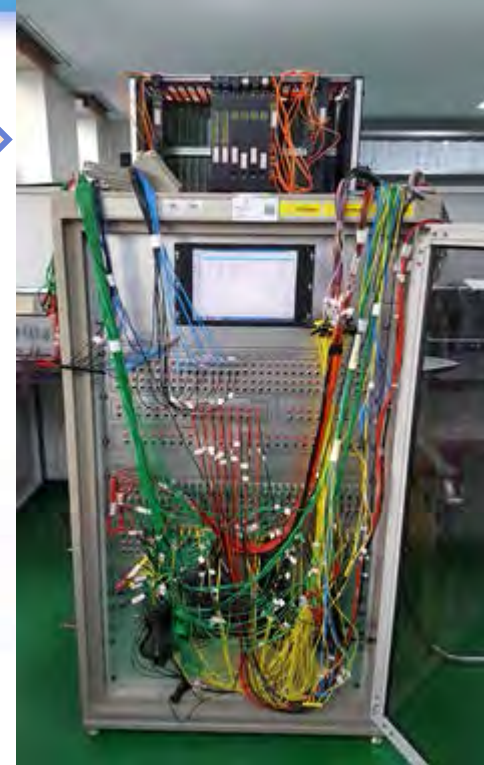
Testing Scenario

$$E = mc^2$$

Integration Test



Target FLC



System Test

DEMO

Status Monitoring Screen

1. I/O Stimulator Platform Qualification

- $Y=aX$ Linear Function, 10,000 test case, Full Scale

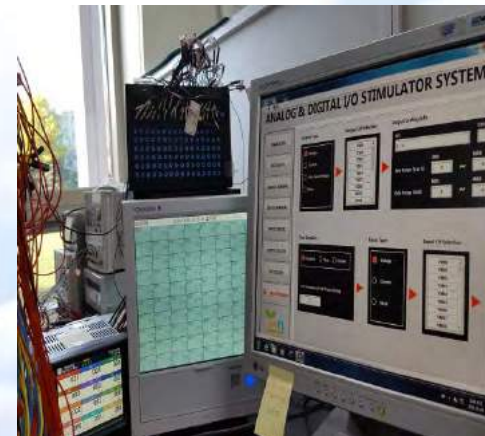
3. Pre-Qualification by Manual

- Fluke 754
- 1st REC, 2nd REC

4. Scenario based Input/Output Automatic Test

- o FAI-> Internal Bus->FPM01-> FDL-> FAO
- o FDI-> Internal Bus->FPM01-> FDL-> FDO
- o FAI-> Internal Bus->FPM01-> FDL-> FDO (cross)
- o FDI->Internal Bus-> FPM01-> FDL-> FAO
 - (Triangle : 0-Rising-Falling-0 : 10,000 Test Case, 200ms, 01.%)

5. Test Result and Analysis



1st REC
2nd REC

System Test for FLC



Target FLC

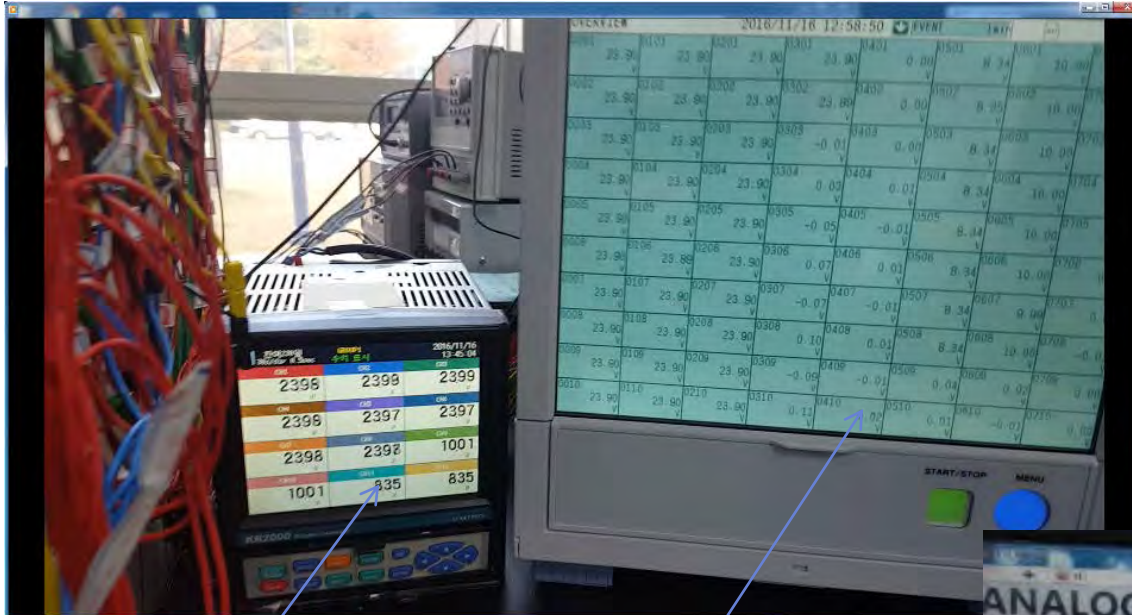


Automatic Signal Generator
– Manual Test
– Automatic Test by initiating Manual

Test Result
– Pass/Fail
– Real-time Performance

Automatic Test Results (Sample)

External Measurement



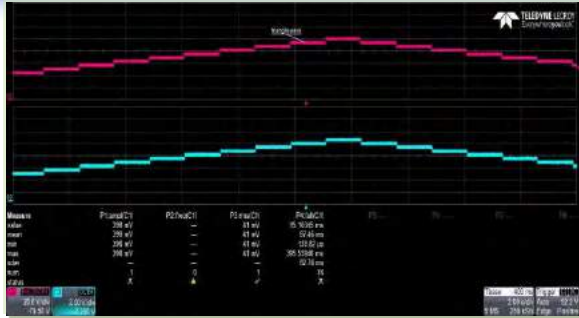
FPM-02

FPM-01

Internal Measurement :
Pass/Fail Decision by timing parameter

ANALOG I/O	Frequency No.	Date	Time	CO Selection	DO Selection	WaveNo	Unit/Qty
	2361	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2362	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2363	2016-11-18	12:58:50	2# 11000	1000	1000	10000
DIGITAL I/O	2364	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2365	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2366	2016-11-18	12:58:50	2# 11000	1000	1000	10000
ANALOG MANUAL	2367	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2368	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2369	2016-11-18	12:58:50	2# 11000	1000	1000	10000
DIGITAL MANUAL	2370	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2371	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2372	2016-11-18	12:58:50	2# 11000	1000	1000	10000
INPUT STATUS	2373	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2374	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2375	2016-11-18	12:58:50	2# 11000	1000	1000	10000
OUTPUT STATUS	2376	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2377	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2378	2016-11-18	12:58:50	2# 11000	1000	1000	10000
TEST STATUS	2379	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2380	2016-11-18	12:58:50	2# 11000	1000	1000	10000
	2381	2016-11-18	12:58:50	2# 11000	1000	1000	10000

Test Results(Real-time)

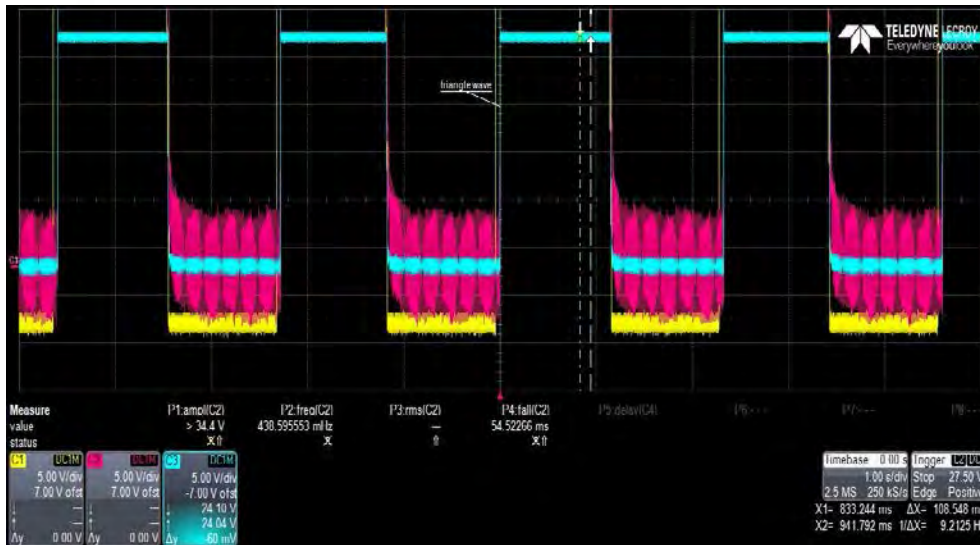
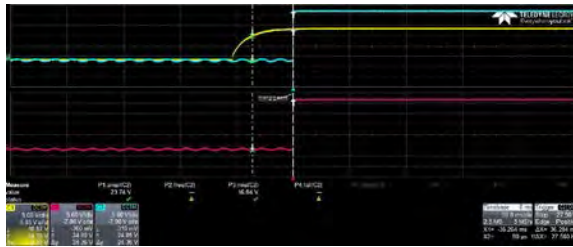


Triangle Wave

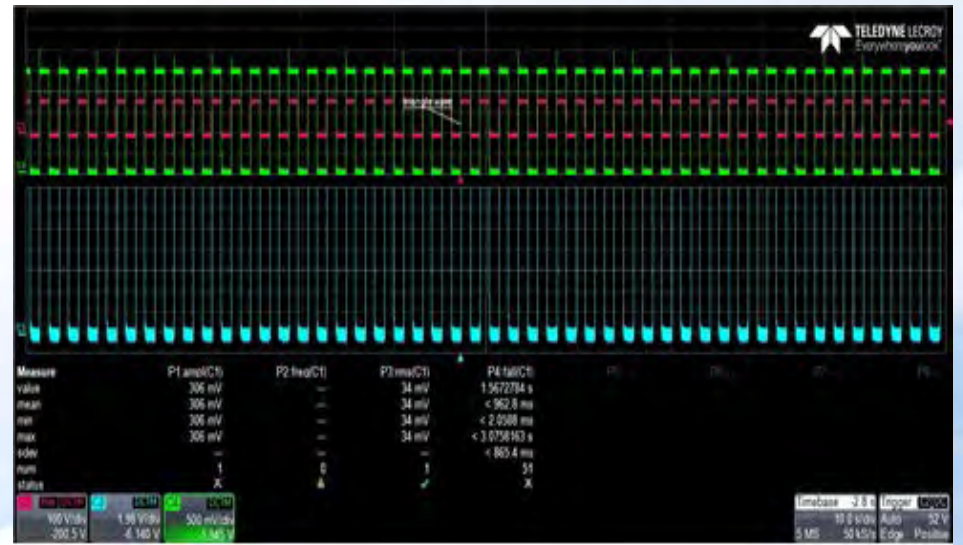


Real-time Performance

Conversion Time Trend (Cross)



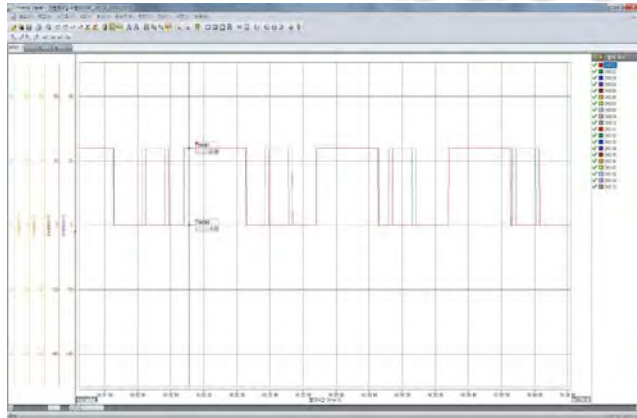
Precision



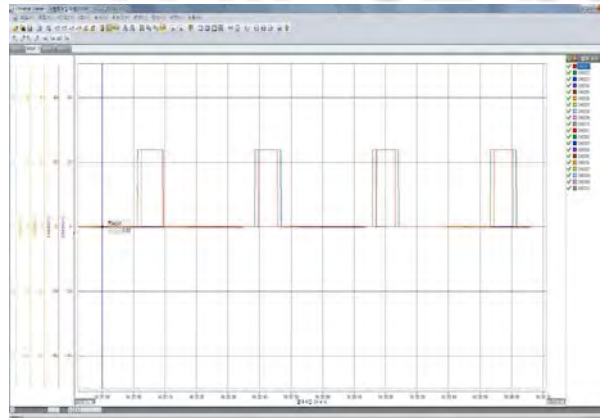
Timing Analysis

Static Analysis of Test Result : FPM-01 based & FPM-02 based

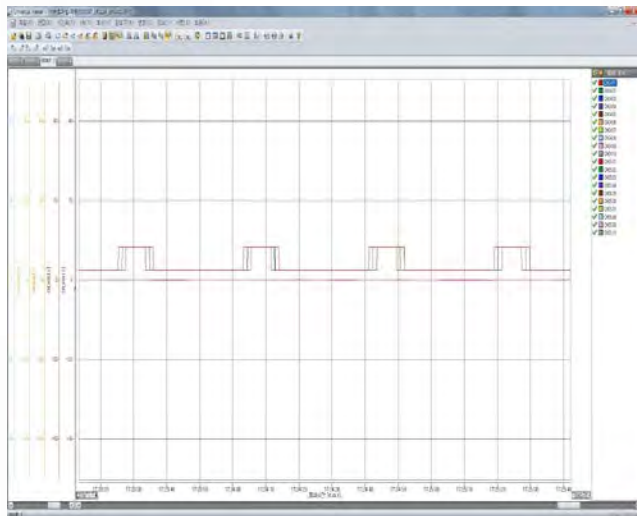
$$E = mc^2$$



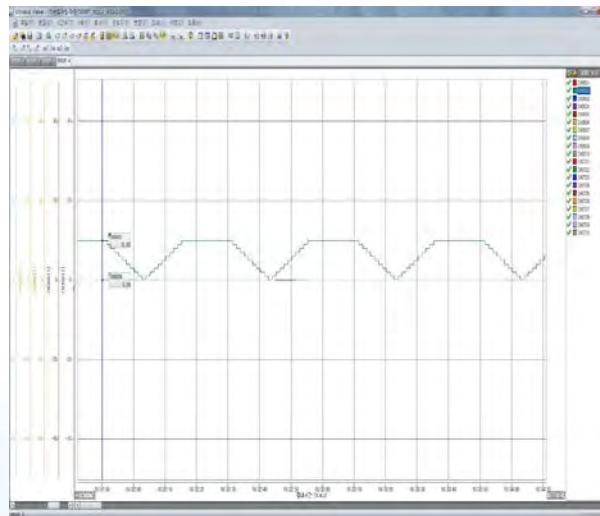
FAI->FDL->FDO, (FDI-> FDL-> FDO)



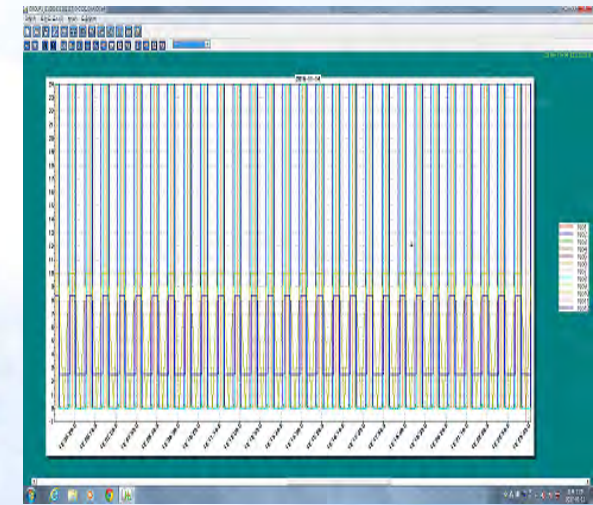
FDI-> FDL-> FDO



FDI-> FDL-> FAO



FAI-> FDL-> FAO



All(FAI-> FDL-> FDO,FDI-> FDL-> FDO, FDI-> FDL-> FAO, FAI-> FDL-> FAO)

Licensing Suitability : Compliance Check

부록 A: IEC Std 7-4.3.2-2003 만족여부

Section	Title	IEEC Std 7-4.3.2-2003 요건 요약	Compliance	Comments
1.	Scope
2.	References
3.	Keyword
4.	안전계통 설계기준	IEEC Std 603-1998의 해당요건을 만족해야 한다.
5.	안전계통 기준
5.1.	단일고장기준	IEEC Std 603-1998의 해당요건을 만족해야 한다.
5.2.	보호조치단절	IEEC Std 603-1998의 해당요건을 만족해야 한다.
5.3.	종말

Section	Title	IEEC Std 7-4.3.2-2003 요건 요약	Compliance	Comments
5.3.1.	소프트웨어 개발	1. 컴퓨터 소프트웨어는 IEEE/IEA 1181에 만족하는 승인된 소프트웨어 플랫폼, 수정 또는 승인되어야 한다. 2. 소프트웨어 개발모듈에는 컴퓨터에 내재되어 있는 모든 프로시저, 소프트웨어 개발보증 계획 제 60880(1986-09) 및 IEC Std 730 있다.
5.3.1.1.	소프트웨어 품질측정	소프트웨어 품질 측정이 이루어질 때 별도 특성들이 고려되어야 한다. -정확성/안정성 (요건단계) -요건의 만족 (설계단계) -설계의 만족 (구현단계)
4.2.1.A.	응답시간	응답시간은 100 msec 이하이어야 하고 다음 사항들을 포함하여야 함. 1. 밀티플 시간. 2. 입력모듈에서의 디지털 신호 변환 시간. 3. Main processor가 PLC 버스를 통하여 입력 값을 습득하는데 걸리는 시간. 4. 2000개 정도의 단순 논리요소를 포함하는 응용프로그램의 2번 스캔에 소요되는 시간. 5. Main Processor가 PLC 버스를 통하여 출력모듈로 데이터를 전송하는 시간. 6. 출력모듈이 버스를 통하여 수신된 디지털 데이터를 해당하는 출력신호형태로 변환하는 시간. 7. 이중화 프로세서의 동기화, 프로세서간의 통신 관련 알고리즘들의 실행을 포함하는 이중화 기능 수행 및 자기감지에 필요한 최대시간.	만족	<ul style="list-style-type: none"> 이날로그 입력력, 디지털 입력력에 대한 응답 시간은 50ms 이하로 요건을 만족함. 데이터링크 통신을 포함한 이날로그 입력력, 디지털 입력력에 대한 응답 시간은 100ms 이하로 요건을 만족함. PLC 기반 안전등급 제어가 설계 사양서 참조. PLC 기반 안전등급 제어가 기능 및 성능 시험보고서 참조. (제외사항) 1. 이중화 프로세서는 사양에 적용하지 않음.
4.2.1.B.	Discrete I/O 수량	PLC는 최소 400 포인트의 discrete I/O를 수용할 수 있어야 함.	만족	<ul style="list-style-type: none"> 디지털 입력력모듈은 각각 2개 채널을 지원하고 하나의 서브모듈에 20개의 모듈 장착 가능함(프로세서모듈 용 한 개 slot 제외). PLC 기반 안전등급 제어가 설계 사양서 참조.
4.2.1.C.	Analog I/O 수량	PLC는 최소 100 포인트의 analog I/O를 수용할 수 있어야 함.	만족	<ul style="list-style-type: none"> 이날로그 입력력모듈은 각각 8개 채널을 지원하고 하나의 서브모듈에 20개의 모듈 장착 가능함(프로세서모듈 용 한 개 slot 제외). PLC 기반 안전등급 제어가 설계 사양서 참조.
4.2.1.D.	조합 I/O 수량	PLC는 최소 50개의 analog 포인트와 400개의 discrete I/O 포인트를 수용할 수 있어야 함.	만족	<ul style="list-style-type: none"> 50개의 이날로그 포인트 지원을 위해서는 7개의 이날로그 입력력모듈이 필요함, 400개의 디지털 포인트 지원을 위해서는 13개의 디지털 입력력모듈이 필요함.

Section	Title	IEEC Std 7-4.3.2-2003 요건 요약	Compliance	Comments
1.2	Use of Standards	IEC 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000
2.	Narrative references
3.	Terms and definitions
4.	Symbols and abbreviations
5.	프로젝트 설명서
5.1.	일반
5.2.	수명 사이클
5.3.	PLC 프로젝트 관리
5.3.1.	일반
5.3.1.1.
5.3.1.2.
5.3.1.3.
5.3.1.4.

Conclusions



- ◉ **QA/SQA/SCM**
- ◉ **COTS Dedication/Tool
Quality Evaluation**
- ◉ **SA**
- ◉ **SVV : Independent Testing**
 - ❖ **Automatic Testing!!!**

Future Plans



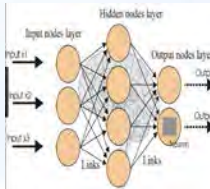
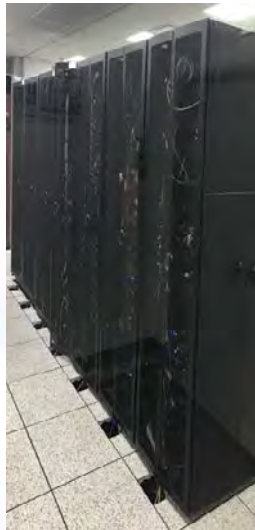
- o Sensors
 - Press
 - Level
 - Temp
 - RTD
 - Bimeta
 - Relay



Clouds/Cluster



IoT+AI



Producing Verification Data