Doosan Heavy Industries & Construction

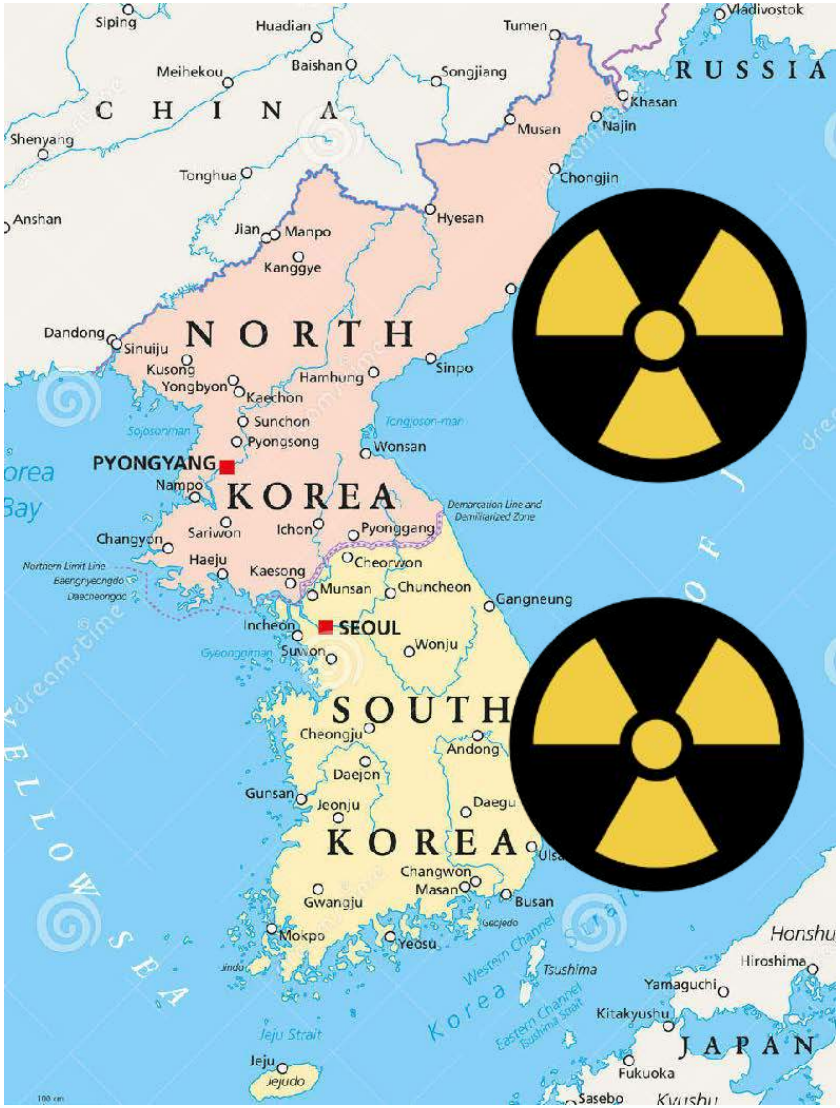
DOOSAN "DFLC-Q" Development

Class 1E FPGA-based Logic Controller for Nuclear Power Plants

12/04/2017

Jin-Young Lim

South Korea & North Korea

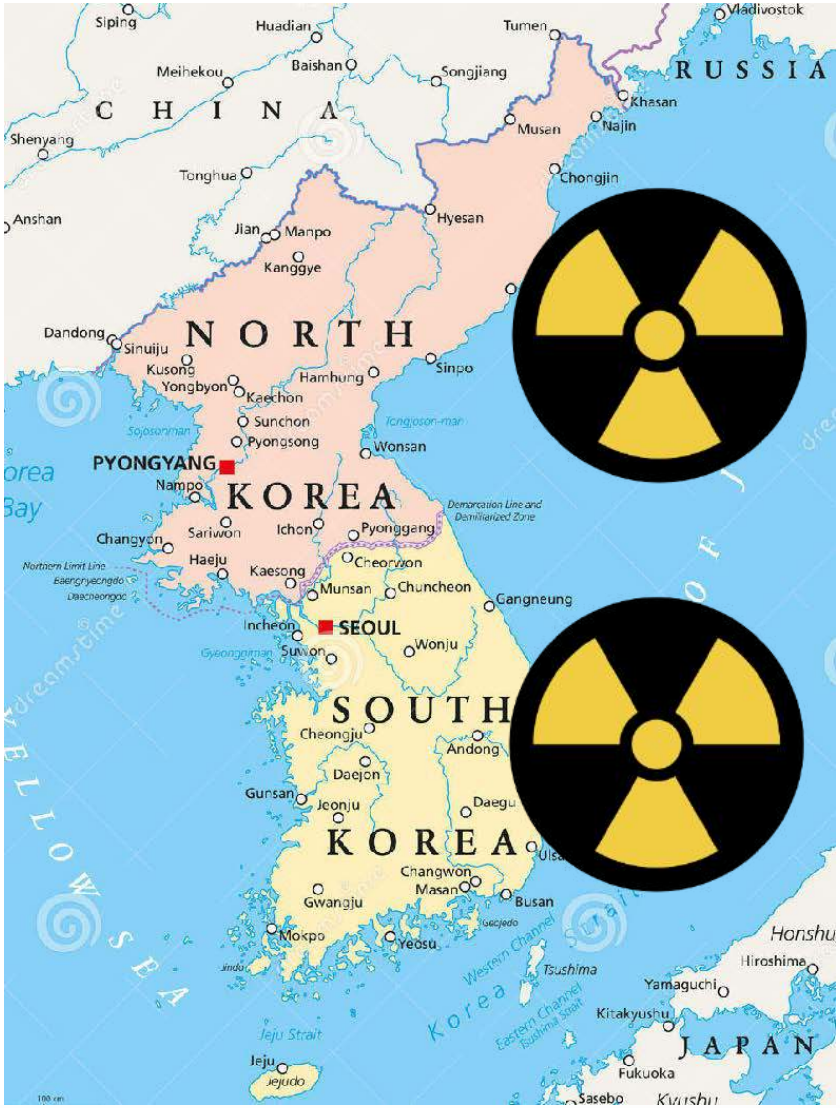


- Nuclear Power ...

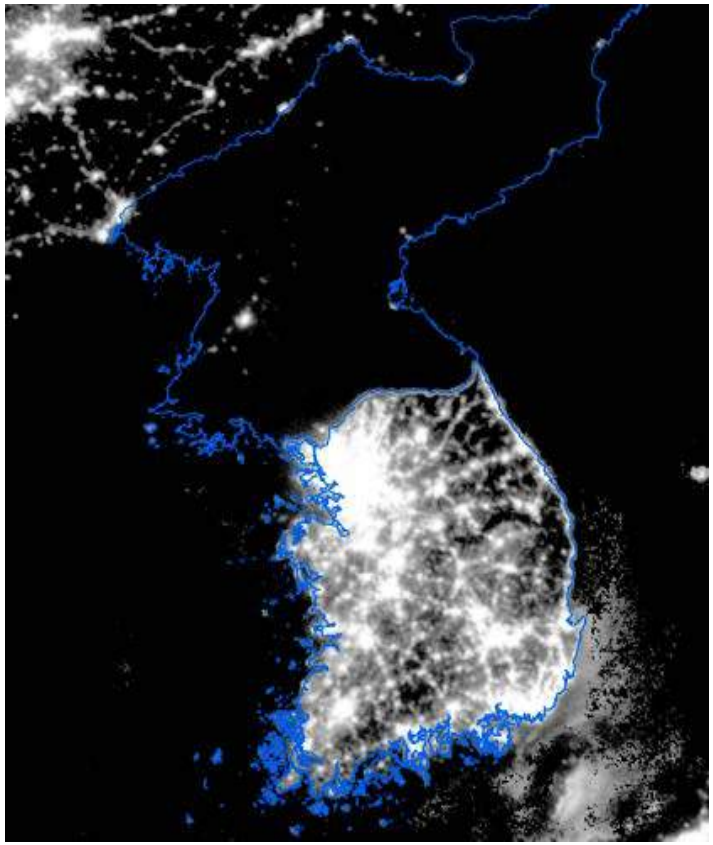
⇒ ***"Dangerous" Bombs ...***

⇒ ***"Safety" Plants !!!***

South Korea & North Korea



- Nuclear Power …

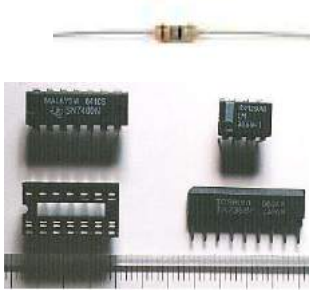


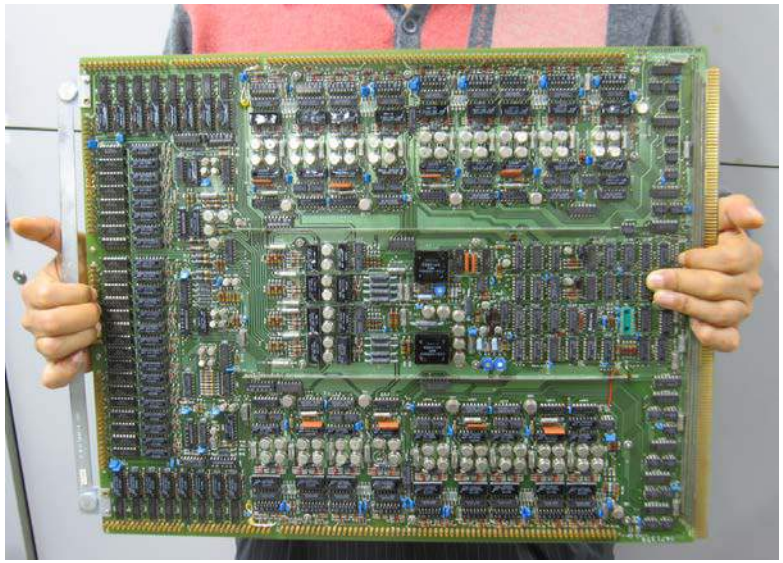
Satellite View at Night…

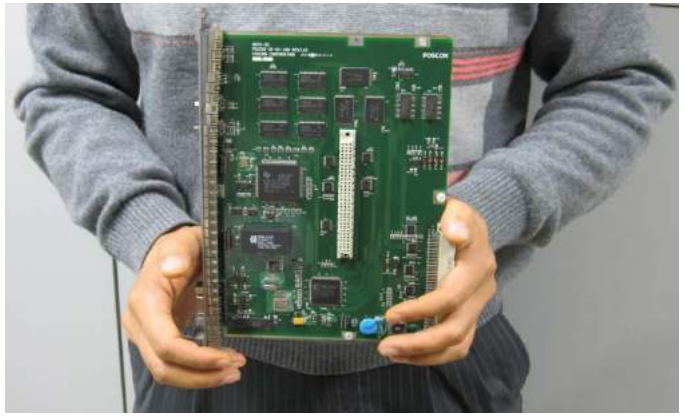
Table of Contents

Background : Technology Trend

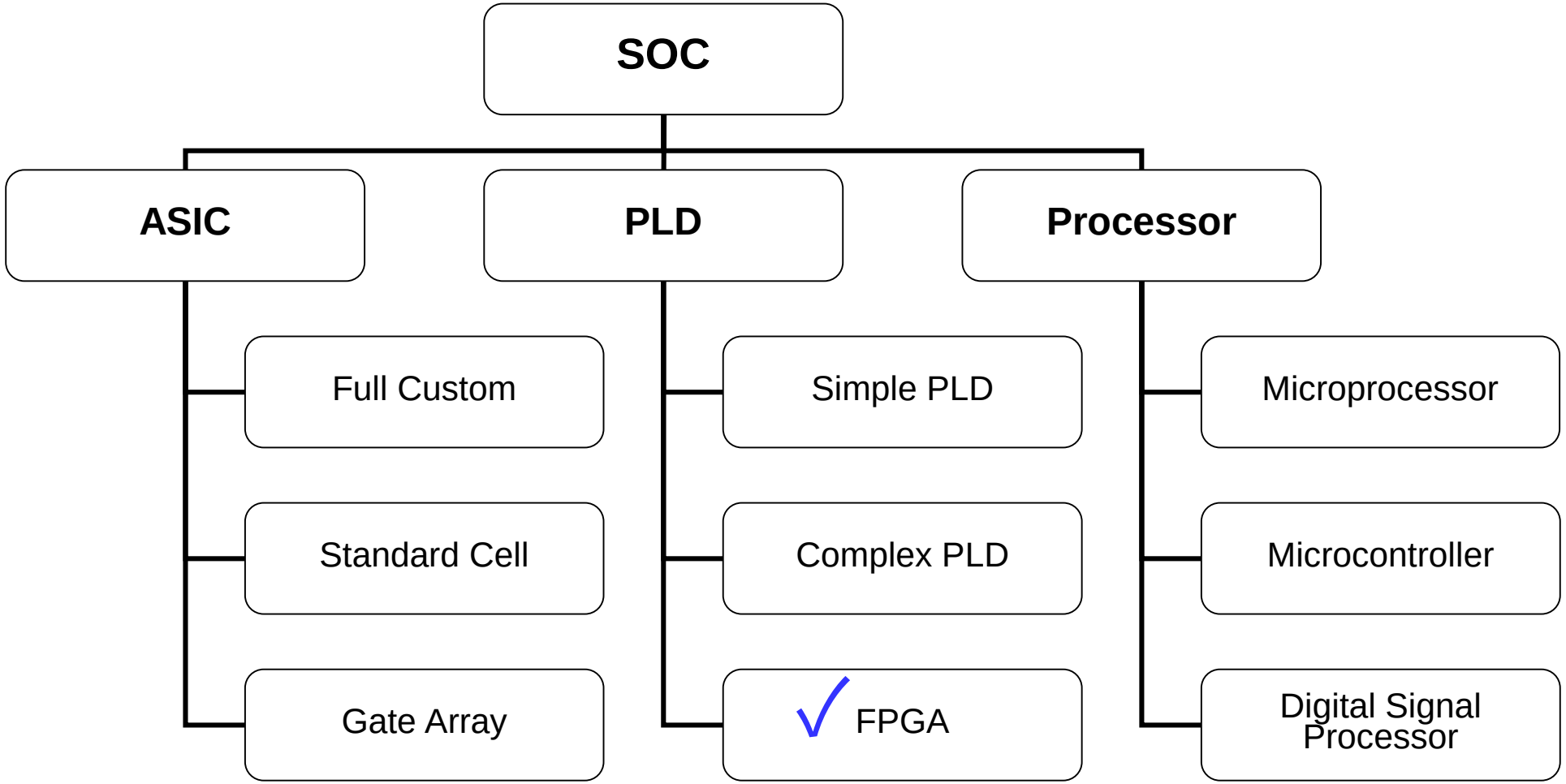
- **Analog System Vs. Digital System**





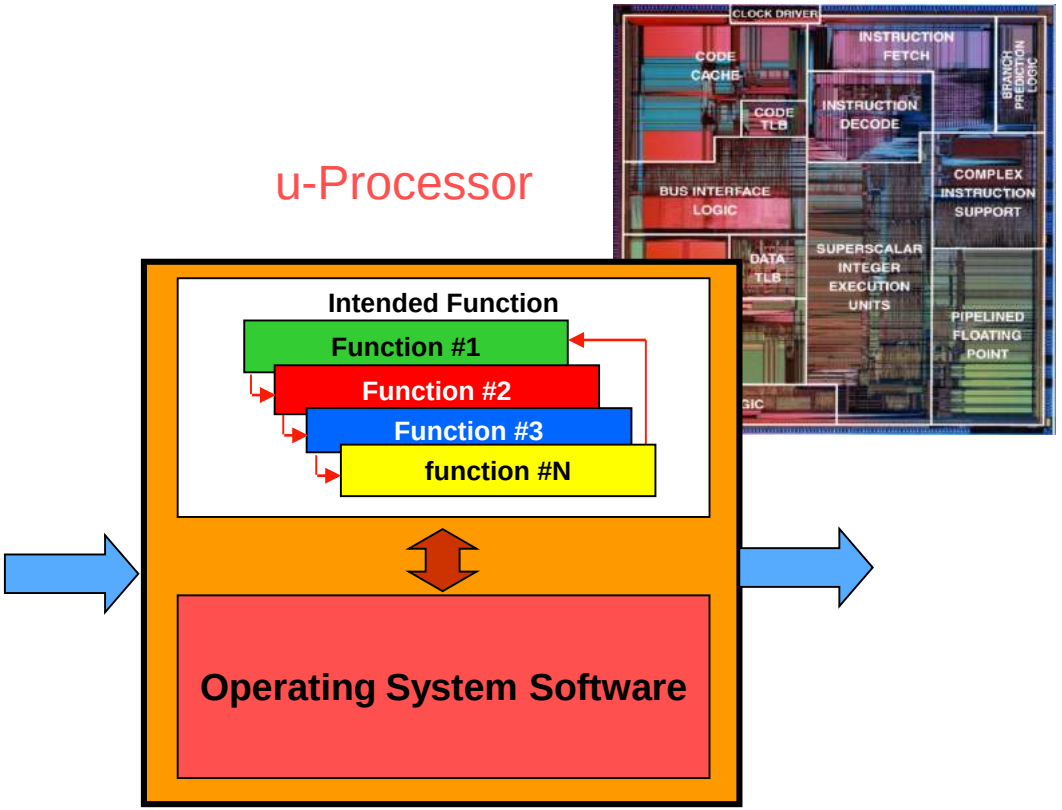


Technology Choice for Digital I&C Design (1)



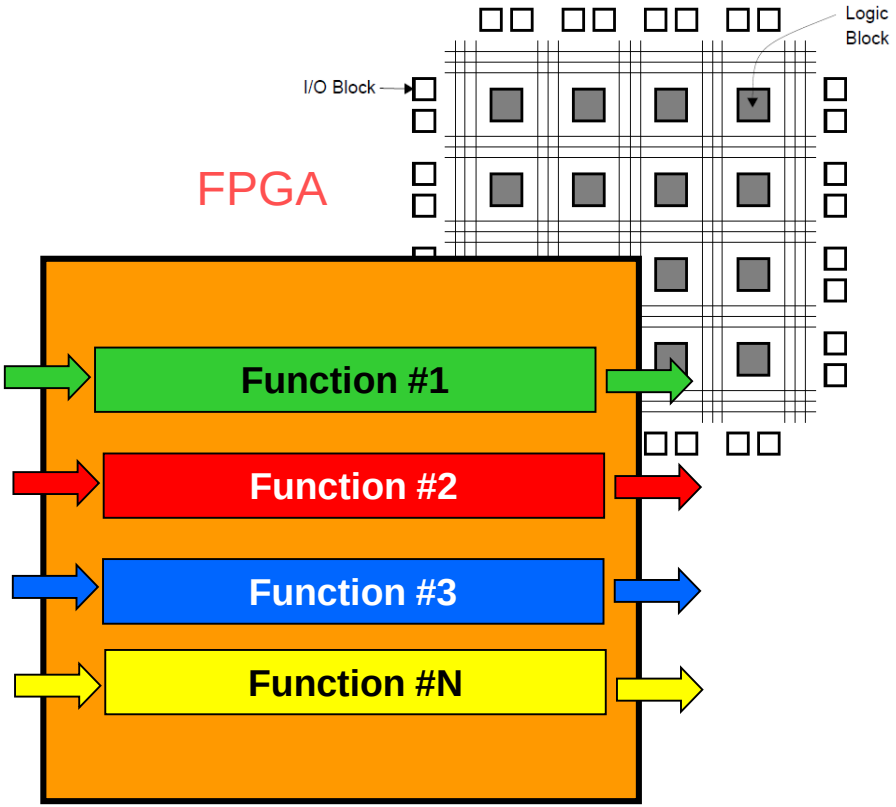
Technology Choice for Digital I&C Design (2)

u-Processor



- Sequential Processing
- Complex Operating System
- Complex middle-ware
- Complex communications software
- Complex maintenance software

FPGA



- Parallel Processing
- No Operating system
- Application logic is directly realized into hardware
- High degree of verifiability
- More deterministic feature

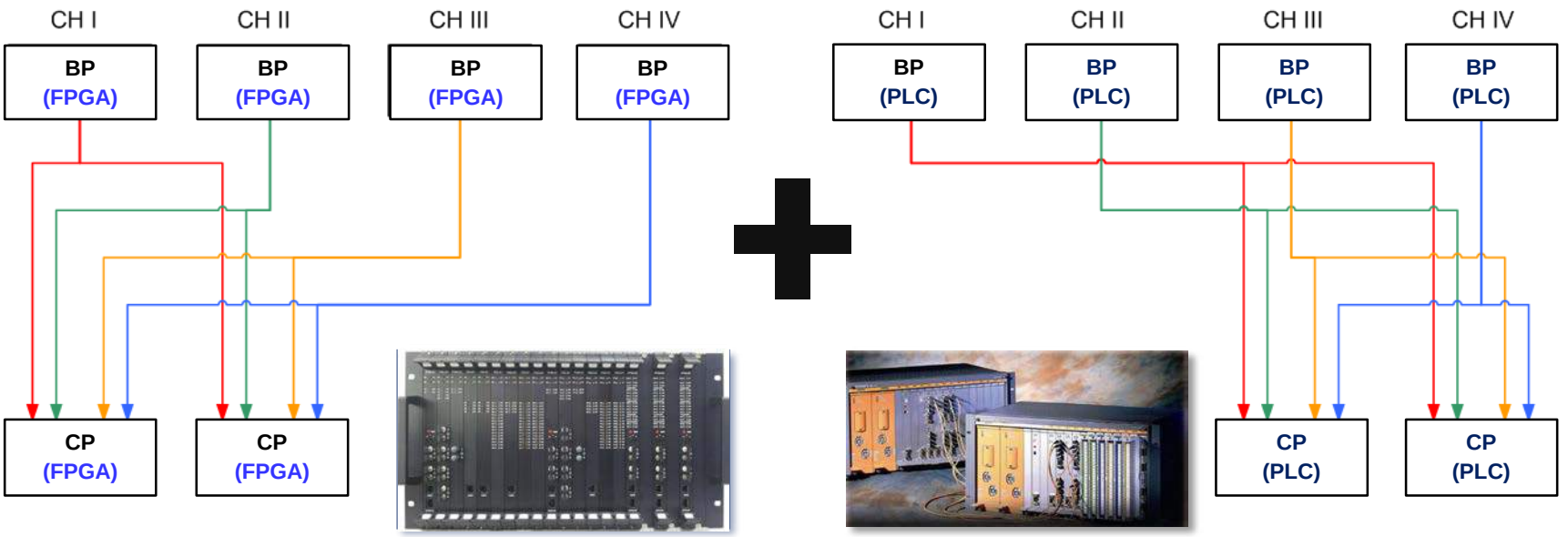
CCF & SPV in Digital I&C system

- **CCF (Common Cause Failure)**
  - Requirements are continuously being increased to make sure safety & reliability of NPP
- **SPV: Single Point Vulnerability**
  - are continuously being removed to enhance the reliability of NPP
- **Required to develop different platform**
  - Launched “Development of safety I&C system and controller against CCF “ by Korean R&D team

DFLC-Q (**D**OOSAN **F**PGA-based **L**ogic **C**ontroller for Class 1E)

Digital I&C Solution against CCF

- **Different Platform of PPS will resolve the CCF Issues**
  - As is – Class 1E Protection System
  - To be – Class 1E independent Protection System using different platform
  - For example) FPGA based PPS and PLC based PPS are using the same time.



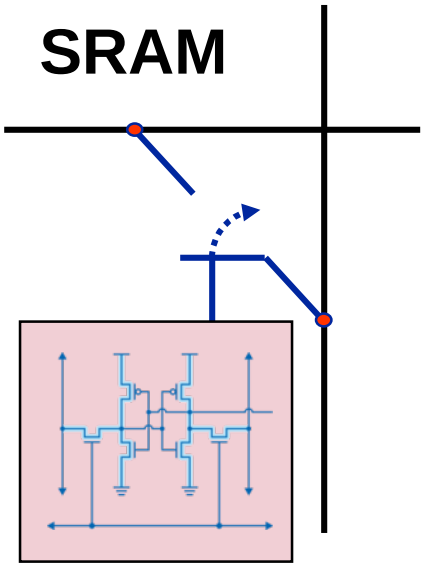
DFLC-Q (FPGA-based Logic Controller)

POSAFE-Q (PLC) (CPU-based Logic Controller)

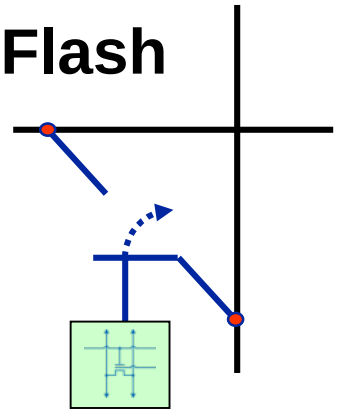
Table of Contents

Technology Choice of FPGA

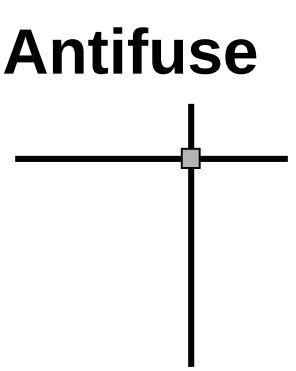
- **FPGA Interconnection Technologies**



Reprogrammable and Volatile



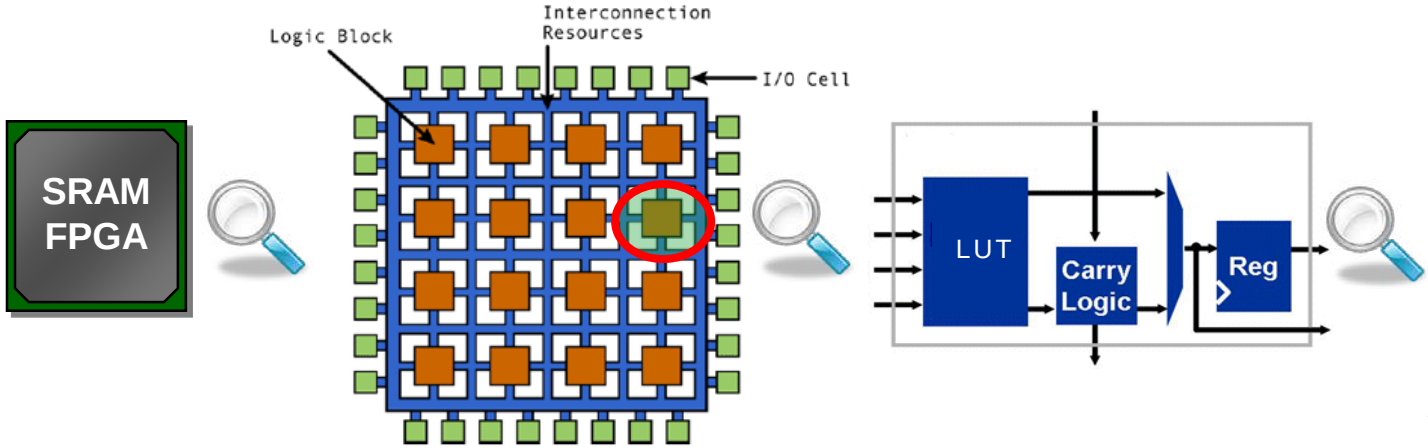
Reprogrammable and Nonvolatile



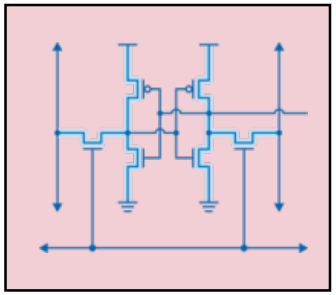
OTP and Nonvolatile

⇒ Concultion-1 :
SRAM FPGA vs. Flash FPGA

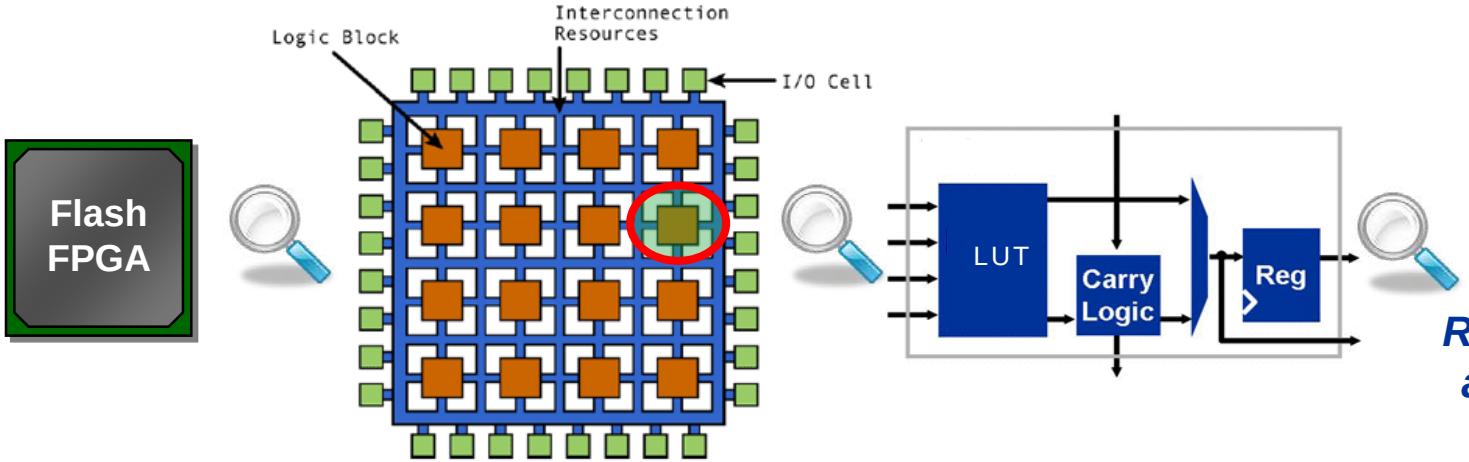
SRAM FPGA vs. FLASH FPGA



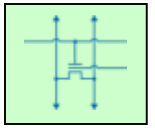
SRAM Cell



Reprogrammable and volatile



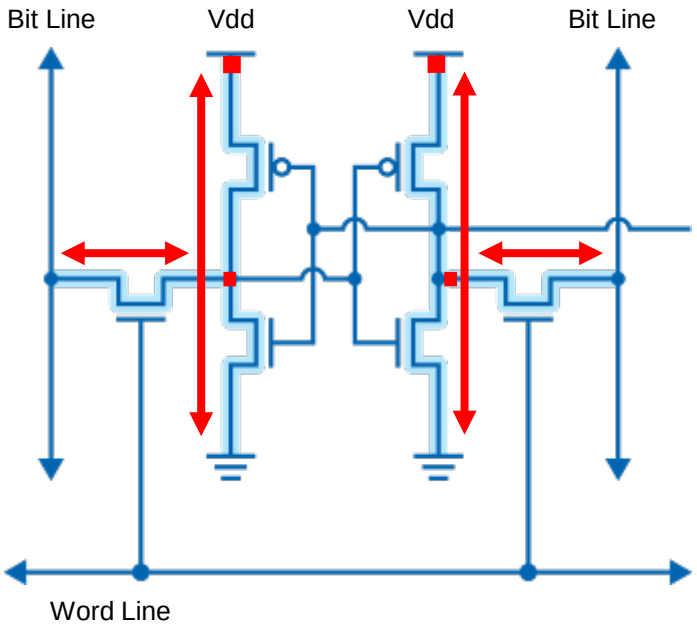
Flash Cell



Reprogrammable and nonvolatile

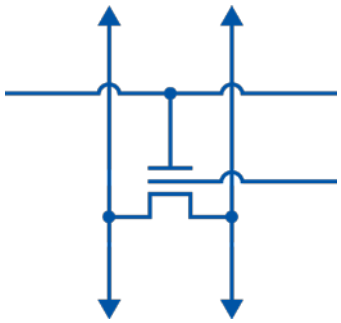
SRAM FPGA vs. FLASH FPGA

Typical SRAM Cell



- High performance
- Millions of Configuration Cells
- Substantial Leakage per Cell
- High Static Current
- ⇒ ***Volatile***

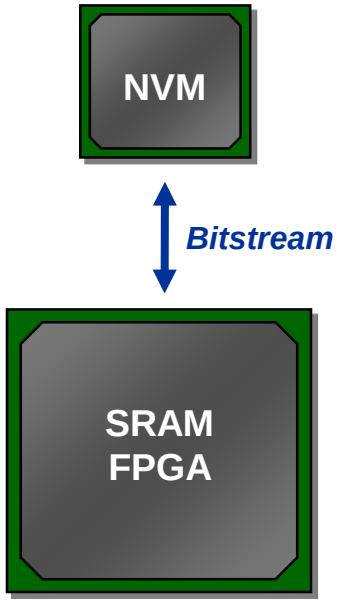
Flash Cell



- Lower performance
- Lower Configuration Cells
- Lower leakage per cell
- Low Static Current
- ⇒ ***Non-Volatile***

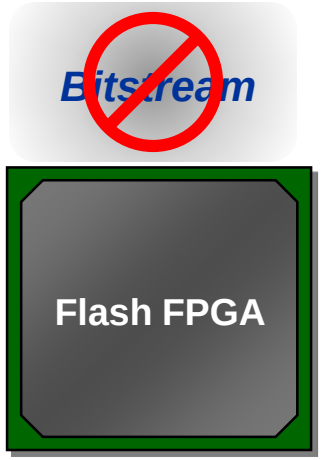
SRAM FPGA vs. FLASH FPGA

SRAM FPGA



Reprogrammable and volatile

Flash FPGA

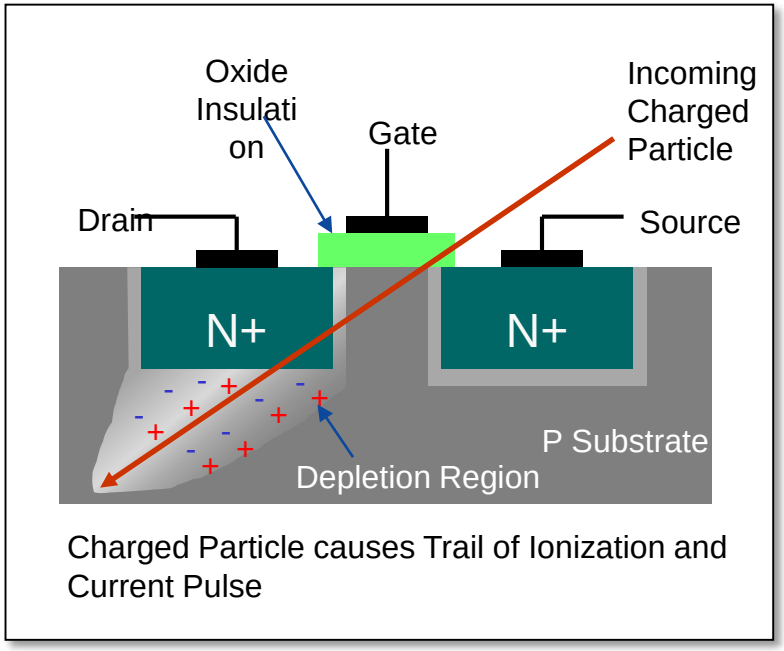


Reprogrammable and nonvolatile

⇒ Concultion-2 : Advantage Flash FPGA

SRAM FPGA vs. FLASH FPGA

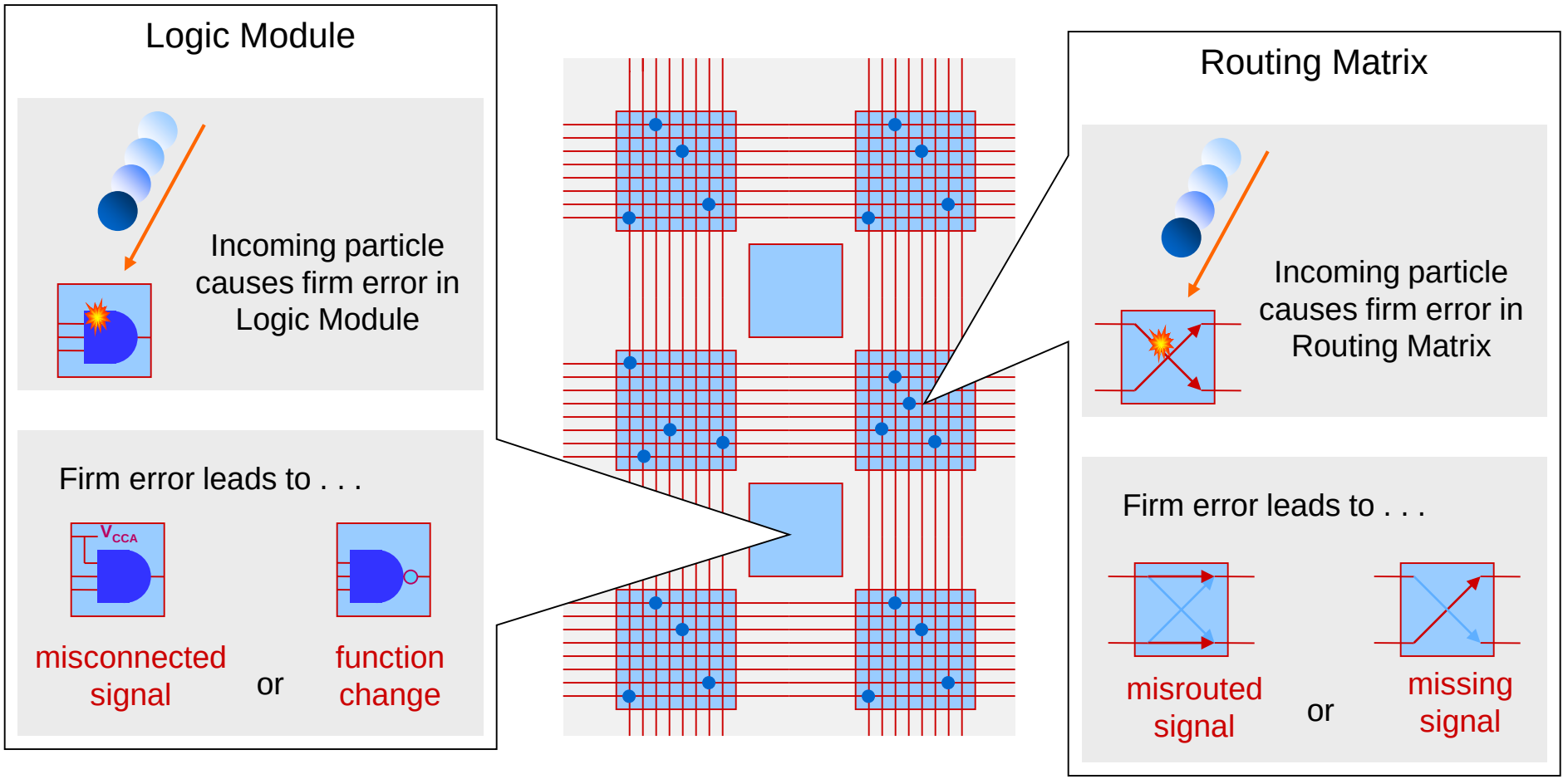
- **Radiation Effects in Semiconductors**
  - Charged particles (alphas, heavy ions, . . .) cause momentary current pulses in CMOS ICs
  - Data in memory cells and flip-flops can change
  - Memory cells and flip-flops are not damaged
  - Industry uses term “soft errors” to describe this process



Charged Particle causes Trail of Ionization and Current Pulse

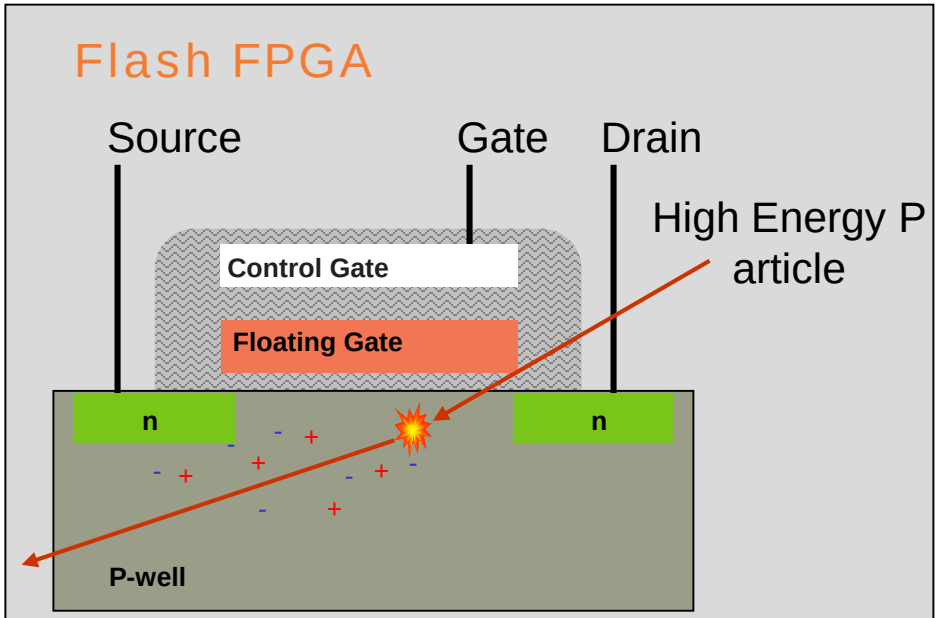
Cofiguration Upset in FPGAs

- **How radiation causes SRAM FPGAS to malfunction**



Flash-based FPGAs – Immune to Configuration Upsets

- Absence of configuration upsets are why Flash-based FPGAs are the Industry Standard for space-flight applications
  - not damaged



High energy particles (atmospheric neutrons, he avy ions in space) cannot generate sufficient cha rge to cause the floating gate to erroneously cha nge state
- True for current generation
- True for next generation

⇒ Concultion-3 : Advantage Flash FPGA

Table of Contents

Development of safety I&C and controller against CCF

- **Korean I&C R&D Project**
  - "Development of safety I&C system and controller against CCF" has been launched to improve the diversity of I&C system

CCF Project

Project 1: Development

- CPU-based Logic Controller (PLC)
- FPGA-based Logic Controller (FLC)
- Reactor Protection System Prototype

Project 2: Validation

- Verification and Validation
- Safety Analysis

FPGA-based Controller

CPU-based Controller

Safety grade I&C System

Overall Activities for Development

Phase 1
(2011 ~ 2013)

- Prototype Developing
  - H/W & Logic Spec.
  - H/W & Logic Design
  - Functional Testing
  - Performance Testing
  - Simplified Qualification Testing

Phase 2
(2014 ~ 2016)

- End Product Developing
  - H/W & Logic Redesign
  - Functional Testing
  - Performance Testing
  - Qualification Testing

DFLC-Q

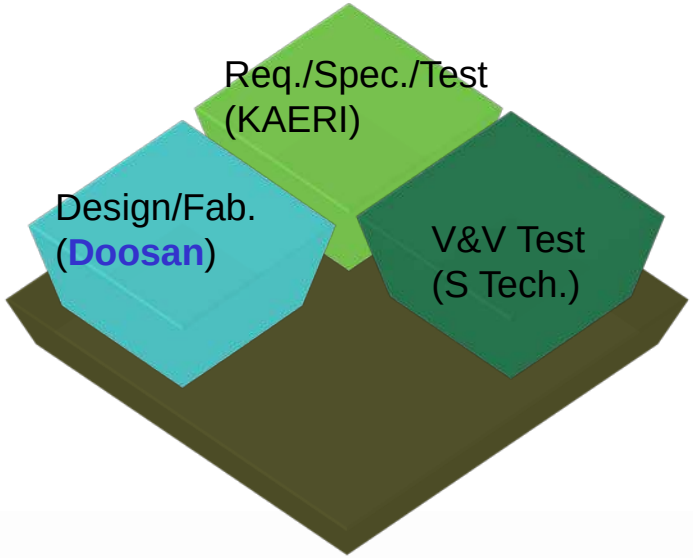
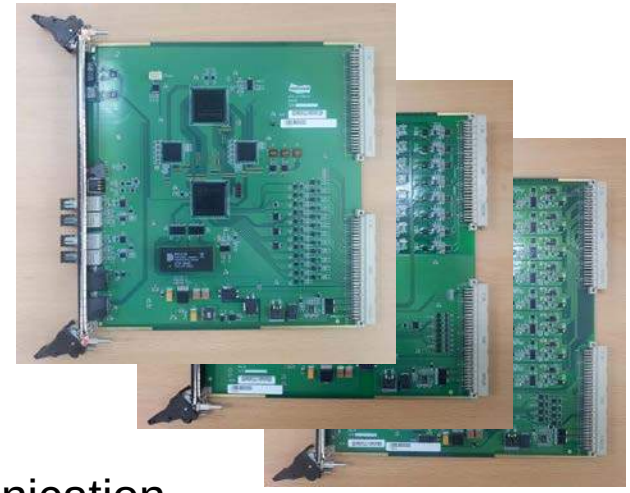


Table of Contents

DFLC-Q [Doosan FPGA-based Logic Controller for Class 1E]

- **Subrack :**
  - 19-inch Standardization (482.6 x 281.35 x 294mm)
  - Total ***21 Slots*** per Subrack
  - Redundant power bus
  - ***Supported 4 system bus groups***

- **Module Type :**
  - Processor Module (Type-I, Type-II)
  - Analog Input Module / Analog Output Module
  - Digital Input Module / Analog Output Module
  - Communication Module
    - Datalink Module for Safety Communication
    - Network / Switch Module for Information Communication



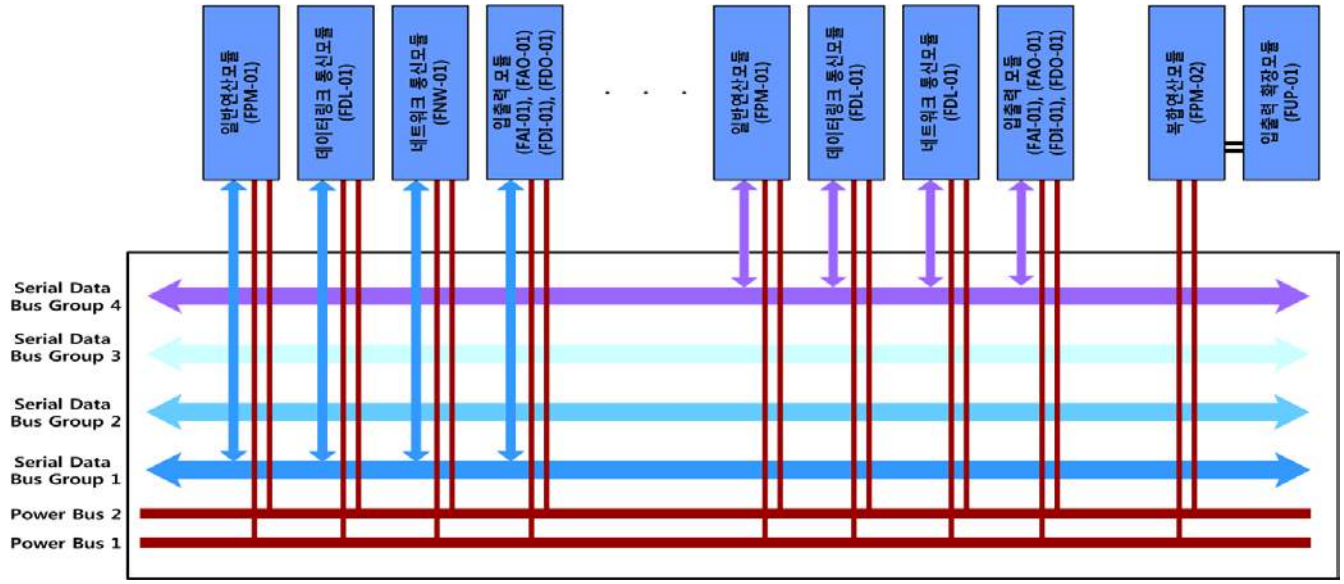
Overall Hardware Specification

Module Type	Item	Specification	Description
Processor Module	Type-I	Control & Application Logic	Embedded Datalink Comm. ports (2-Ch)
	Type-II	Control & Application Logic + Analog / Digital I/O Ch.	Embedded I/O Channel (Support Extension Module)
Analog I/O Module	Range	0V~10V, 4mA~20mA	8-Ch (Current / Voltage)
	Accuracy	±0.1%	18-bit AD / 16-bit DA
	Update Time	Min. 5 msec	w/ PM Scantime
Digital I/O Module	Range	0V ~ 24V	32-Ch
	Update Time	Min. 5 msec	w/ PM Scantime
Datalink Comm. Module	Speed	10-Mbps	4-Ch per Module (Separated Tx / Rx port)
	Protocol	Based on RS-485	
Network Comm. + Netwok Switch Module	Speed	20Mbps / 64-node	1-Ch per Module (Separated Tx / Rx port)
	Protocol	TDMA	

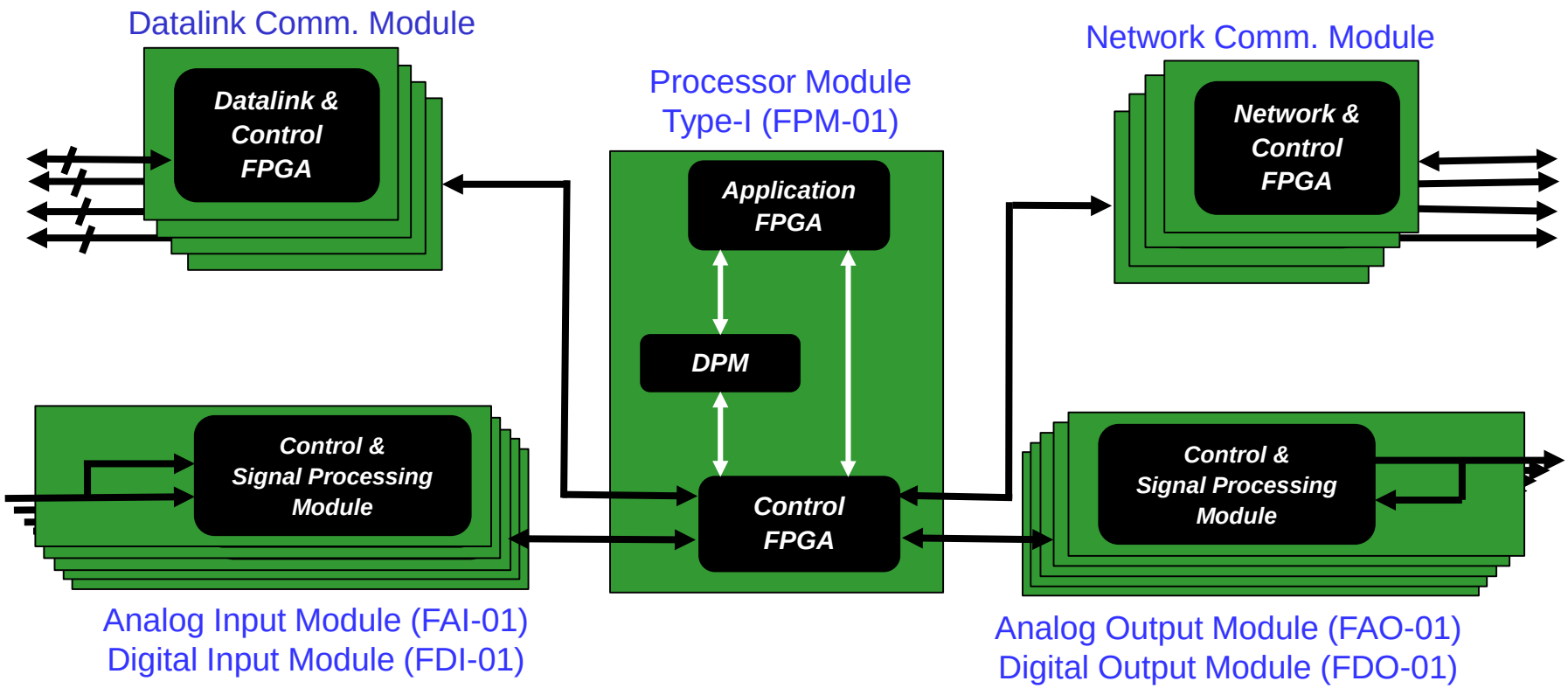
DFLC-Q : System Bus Architecture

- **1-Subrack :**
  - ***"Supported 4 System-Bus-Group***

⇒ Support 4 independent sub-system per subrack

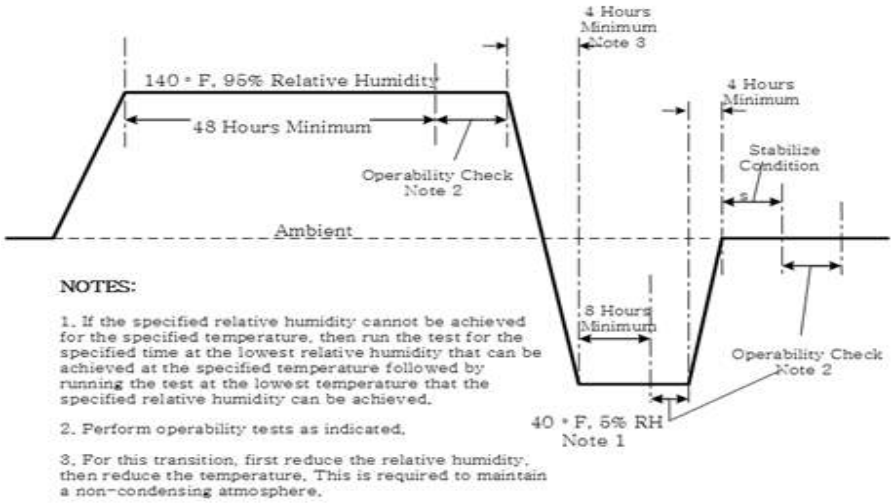


DFLC-Q : System Diagnosis



Equipment Qualification Test(1)

- **Environmental qualification (IEEE Std. 323-2003, Reg. Guide 1.209)**



- **EMI/RFI (Reg. Guide 1.180-2003, IEC 61000-4-2-2008)**

EMI/RFI Emissions

	MIL-STD
Conducted	CE101 CE102
Radiated	RE101 RE102
Baseline	

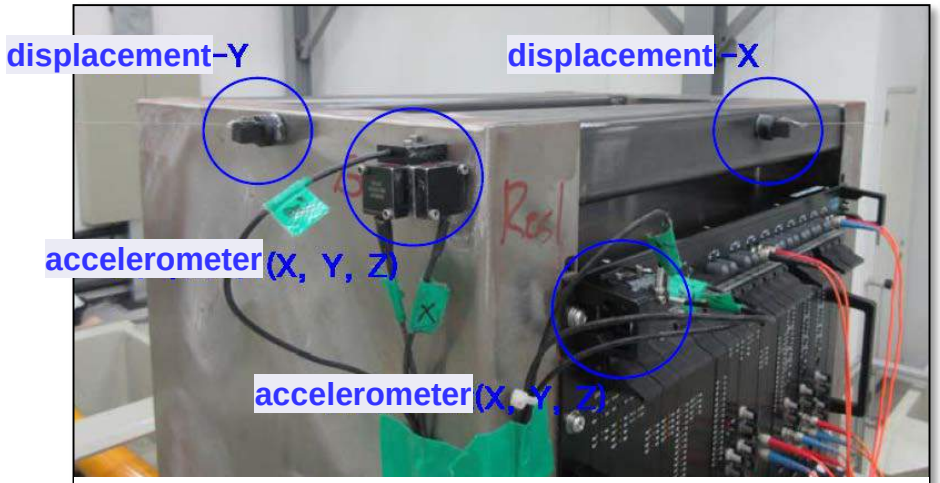
EMI/RFI Susceptibility

	Power	Signal
	CS101 CS114	CS114 CS115 CS116
	RS101(*) RS103	

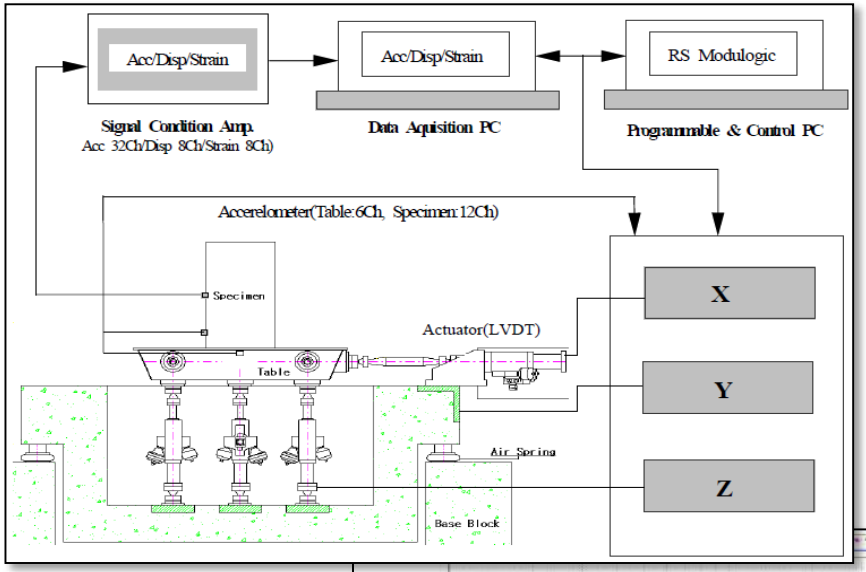
(*) Exemption based on proximity to magnetic field emitters

Equipment Qualification Test(1)

- **Seismic Testing (IEEE Std. 344-2004, Reg. Guide 1.110)**

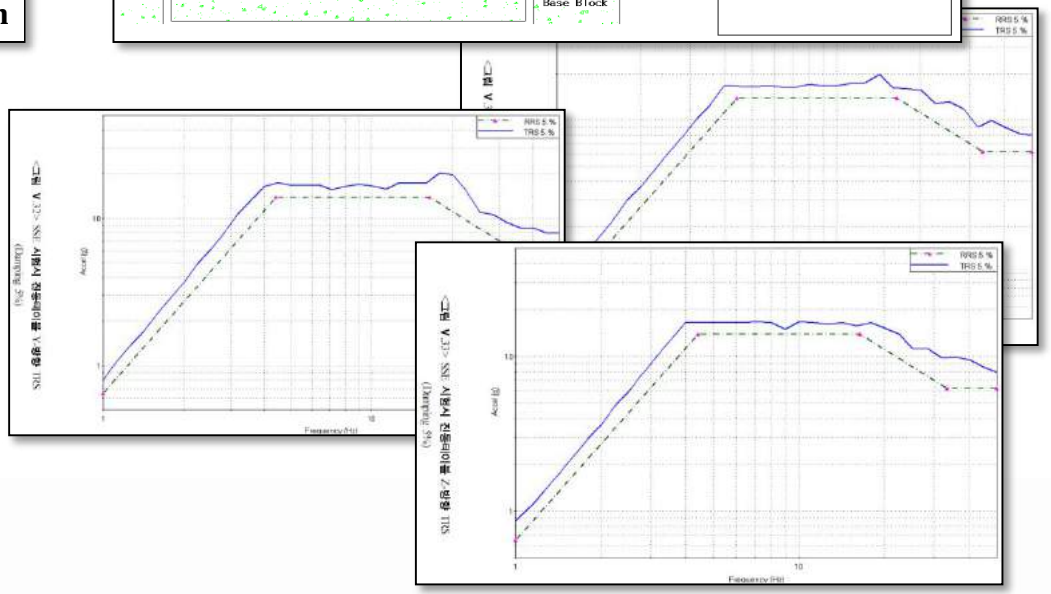


Accelerometers and displacement meter installation location



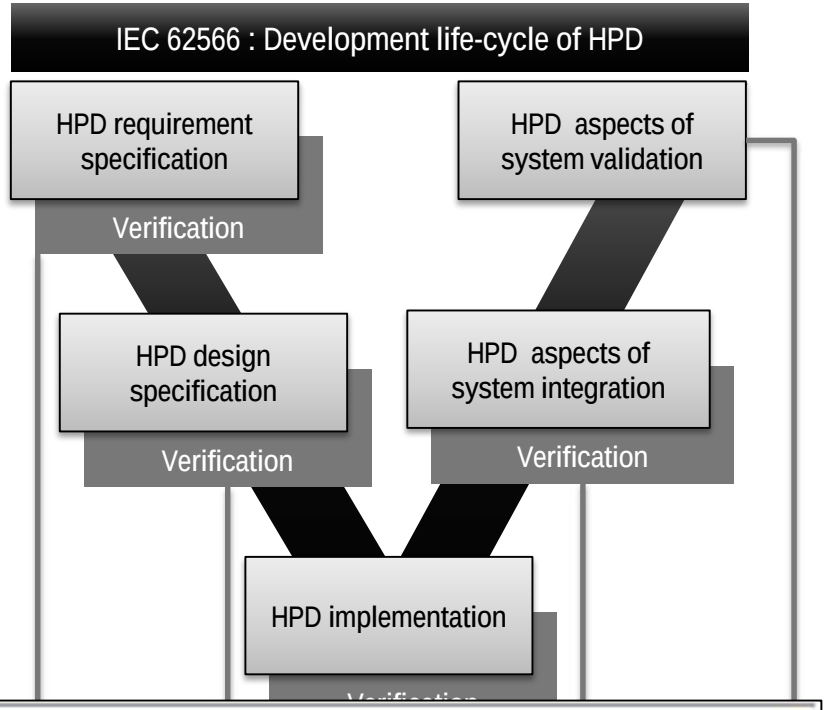
Allowed during seismic testing standards

No	Signal type	Tolerance	Etc.
1	Analog Voltage	5 V ± 0.14%	4 Channel
2	Analog Current	12 mA ± 0.14%	1 channel
3	Digital Voltage	22 ~ 24 VDC	5 channel



Overall development life cycle(1)

IEC 62566 Section 9 HPD Verification	Application Notes
9.1 General	▪ Independent V&V team
9.2 Verification plan	▪ Software V&V plan in the concept phase
9.3 Verification of the use of the pre-developed items	▪ Original software
9.4 Verification of the design and implementation	▪ SRS, SDD document evaluation
9.5 Test-benches	▪ Test-benches to fulfil requirement and path coverage
9.6 Test Coverage	▪ Path/Branch coverage for Component Test ▪ Requirement coverage for Integration Test
9.7 Test Execution	▪ Behavioral simulation using test benches



Day 3 – Wednesday, 6 December 2017

Time	Event	Speaker
Technical Session on Design and Testing		**Chair: Gyula Mach**
09:00 – 9:30	Presentation 10: Verification and Validation of FPGA-Based Logic Controller	Jangyeol Kim, KAERI

※HPD : HDL-Programmed Device

Summary of DFLC-Q Development

- **Against CCF and SPV issues:**
  - ***Using Different platform is the one of the solution***
- **Proposed both FPGA-based and CPU-based Logic Controller**
  - ***Developed both system in the past project***
- **Developed DFLC-Q by DOOSAN**
  - ***Based on Flash-based FPGAs***
- **The Next…**
  - ***Processing to certify DFLC-Q as a Safety-Grade Digital I&C System***

Q & A