DOOSAN

Doosan Heavy Industries & Construction

Doosan Practice of V&V and Testing in FPGA Development Process

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Shanghai, China

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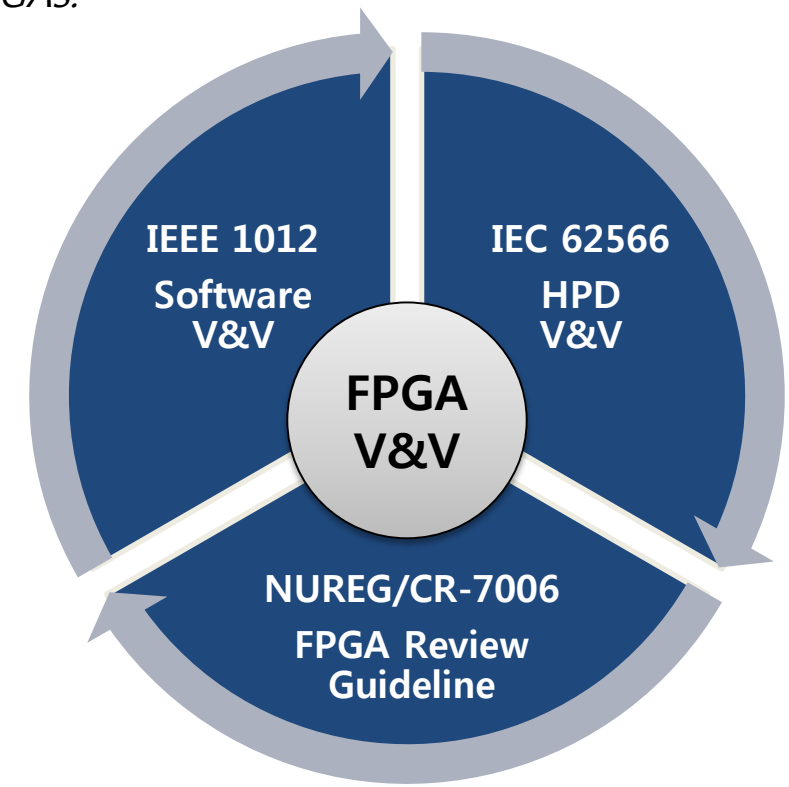
I. Introduction
1-1. V&V in FPGA Development Process

- **FPGA has mixed characteristics of hardware and software**

- **FPGA V&V is hard to be achieved with IEEE Std. 1012 (a basis for NPP software V&V)**
  - *[NUREG/CR-7006] IEEE-1002-2004 is a software-only standard, and it can not be directly applied to V&V process for FPGA-based systems. Even though the top level V&V processes and underlying activities are generic and can be used for FPGAs, the low level tasks are software specific, and not directly applicable to FPGAs.*

➔ **Harmonized existing FGPA standards and technologies into IEEE Std. 1012-based SDLC (Software Development Life Cycle)**

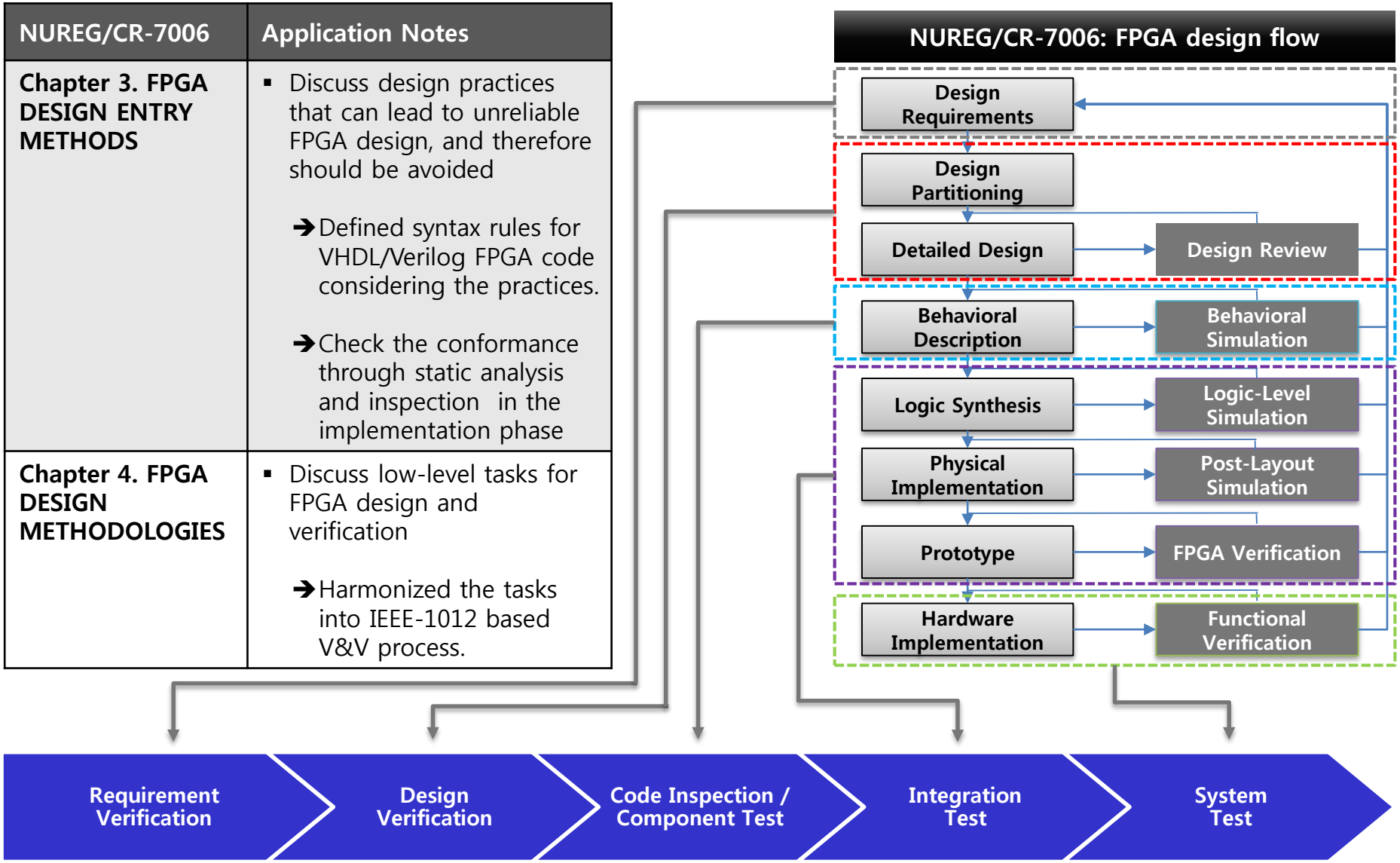
- **IEEE Std. 1012 :** Standard for Software Verification and Validation
- **NUREG/CR-6007 :** Review Guidelines for Field-Programmable Gate Arrays in Nuclear Power Plant Safety Systems
- **IEC 62566 :** Nuclear power plants – Instrumentation and control important to safety – Development of HDL-programmed integrated circuits for systems performing category A functions



I. Introduction

1-2. Application of NUREG/CR-7006 Review Guidelines for FPGA in NPPS

NUREG/CR-7006	Application Notes
Chapter 3. FPGA DESIGN ENTRY METHODS	▪ Discuss design practices that can lead to unreliable FPGA design, and therefore should be avoided ➔Defined syntax rules for VHDL/Verilog FPGA code considering the practices. ➔Check the conformance through static analysis and inspection in the implementation phase
Chapter 4. FPGA DESIGN METHODOLOGIES	▪ Discuss low-level tasks for FPGA design and verification ➔Harmonized the tasks into IEEE-1012 based V&V process.

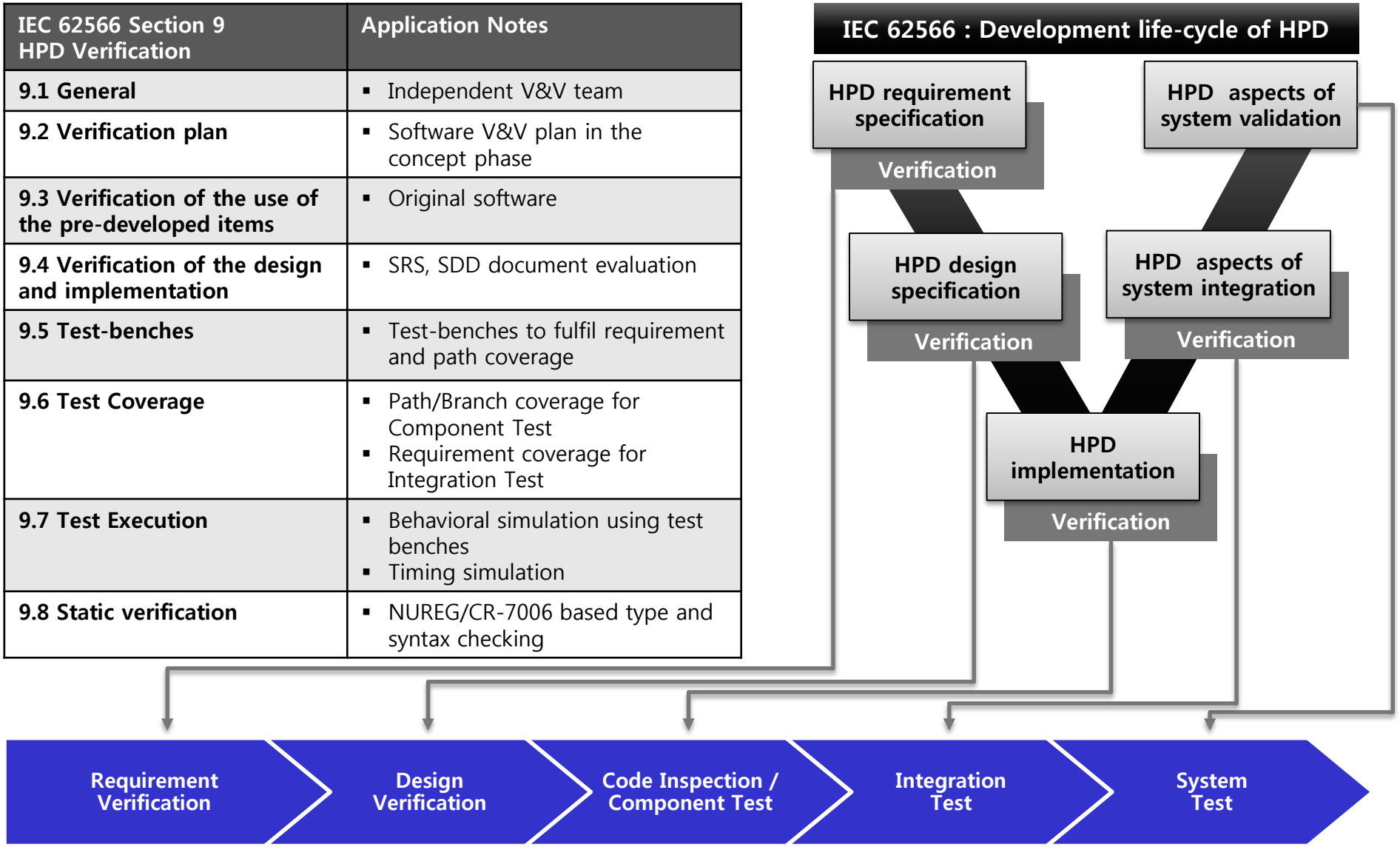


IEEE Std. 1012-based SDLC(Software Development Life Cycle)

I. Introduction

1-3. Application of IEC 62566 : HPD※ Verification

IEC 62566 Section 9 HPD Verification	Application Notes
9.1 General	▪ Independent V&V team
9.2 Verification plan	▪ Software V&V plan in the concept phase
9.3 Verification of the use of the pre-developed items	▪ Original software
9.4 Verification of the design and implementation	▪ SRS, SDD document evaluation
9.5 Test-benches	▪ Test-benches to fulfil requirement and path coverage
9.6 Test Coverage	▪ Path/Branch coverage for Component Test ▪ Requirement coverage for Integration Test
9.7 Test Execution	▪ Behavioral simulation using test benches ▪ Timing simulation
9.8 Static verification	▪ NUREG/CR-7006 based type and syntax checking



※ *HPD : HDL-Programmed Device*

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2. V&V and Testing

2-1. Document Evaluation and Static Verification

➢ **Evaluates design documents and HDL-program code using BTP-14※, IEEE Std. 1012, and NUREG/CR-7006**

SRS/SDS/Code Documentation					Code
BTP-14		IEEE Std. 1012			NUREG/CR-7006
Functional Characteristics	Process Characteristics	Traceability Analysis	Document Evaluation	Interface Analysis	FPGA DESIGN ENTRY METHODS
Accuracy	Completeness	Correctness	Correctness	Correctness	Reliability
Functionality	Consistency	Consistency	Consistency	Consistency	Robustness
Reliability	Correctness	Completeness	Completeness	Completeness	Traceability
Robustness	Style	Accuracy	Accuracy	Accuracy	Maintainability
Safety	Traceability		Readability	Testability	
Security	Unambiguity		Testability		
Timing	Verifiability				

➔ **Verification through inspection and walkthrough using checklist**

※ *USNRC-0800 Standard Review Plan: Chapter 7. Instrumentation and Controls BTP-14*

2. V&V and Testing:Micro-semi(Libero)

2-2. Component Test

Requirement Verification | Design Verification | **Code Inspection / Component Test** | Integration (card, module) Test | System (FPGA controller) Test

- **Behavior/timing simulation was performed on RTL/HDL code**
- **Test criteria : Path coverage, Requirement coverage**
- **Test environment : Host PC-based Simulation Environment**

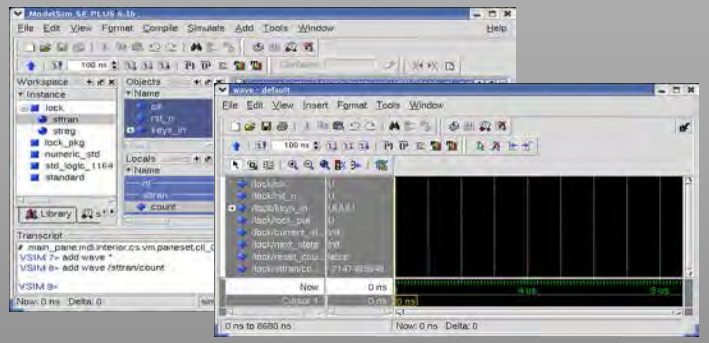
Host PC for Testing

Test Case Simulation Result

STIMULI / Test Input → **Target FPGA Under Test** → **RESPONSE / Test Result**

Test Benches

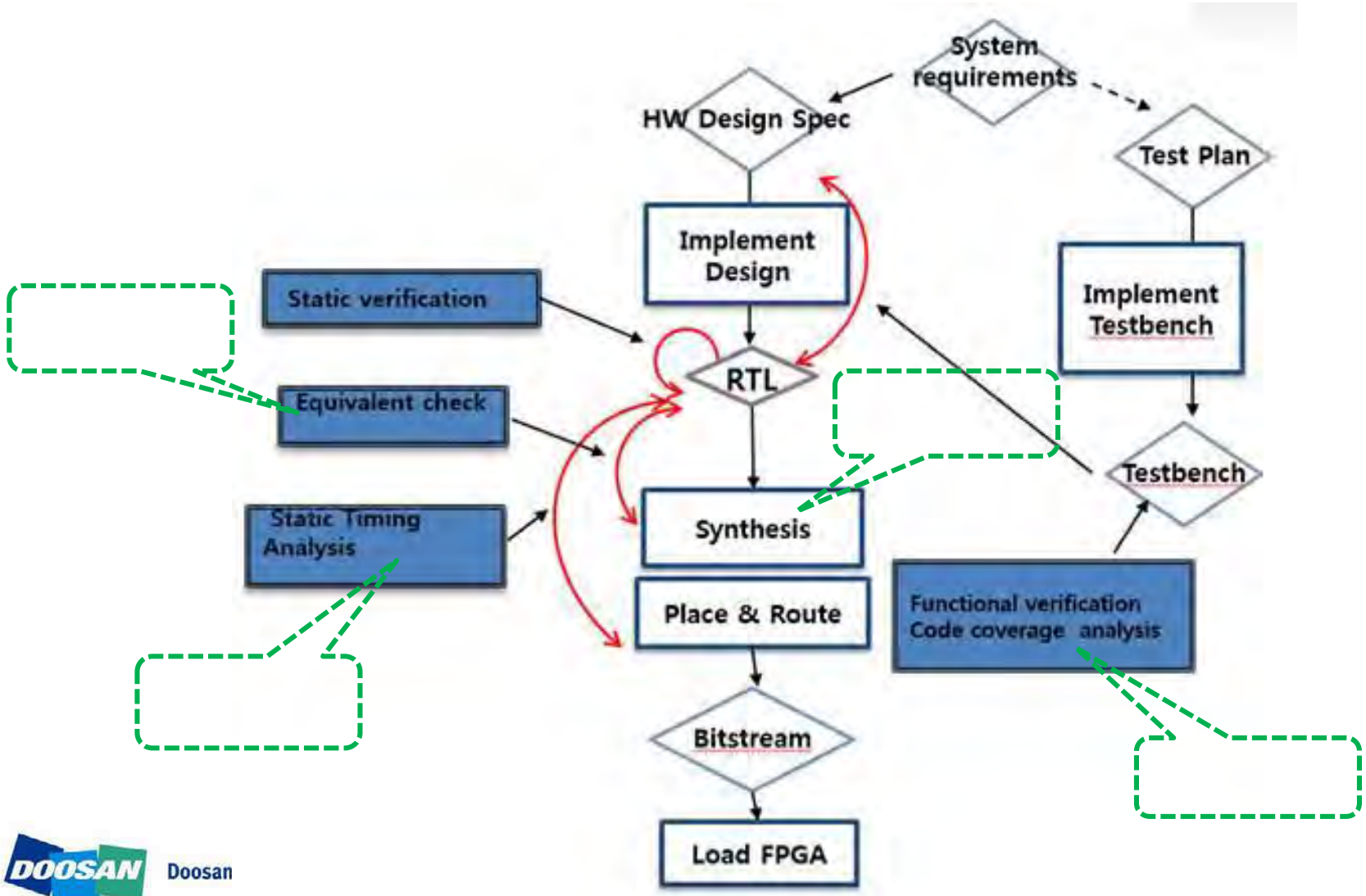
Simulation Environment



Host OS (Windows)

2. V&V and Testing
2-2. Component Test

Requirement Verification | Design Verification | **Code Inspection / Component Test** | Integration (card, module) Test | System (FPGA controller) Test



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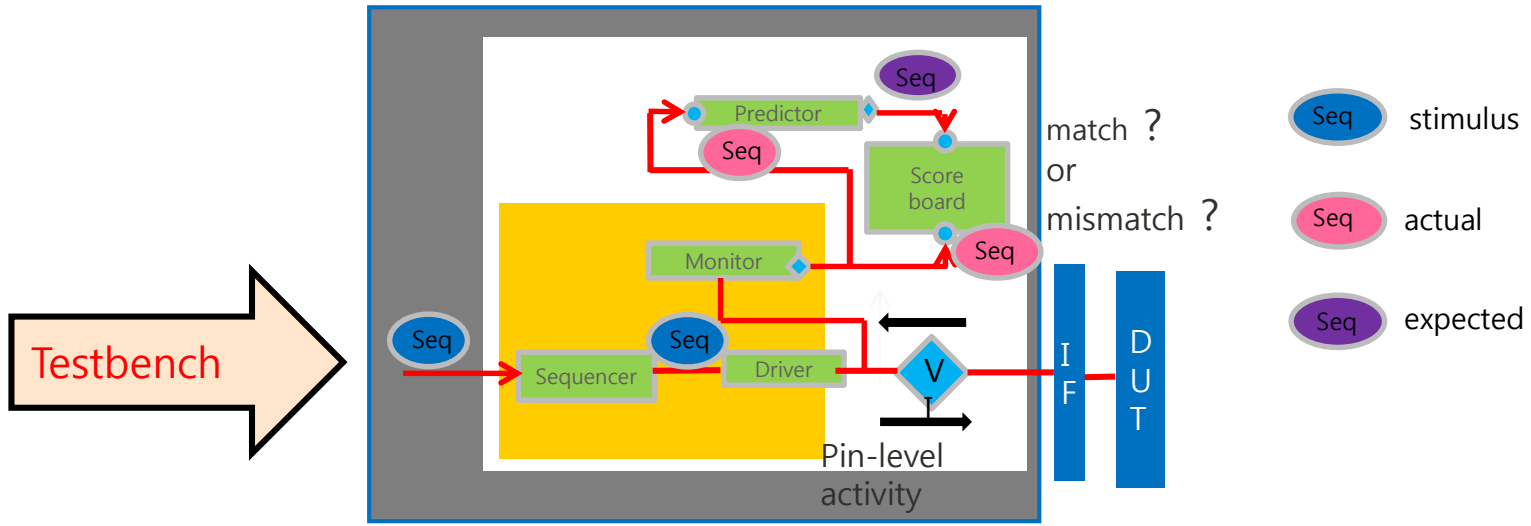
2. V&V and Testing
2-2. Component Test

Requirement Verification | Design Verification | **Code Inspection / Component Test** | Integration (card, module) Test | System (FPGA controller) Test

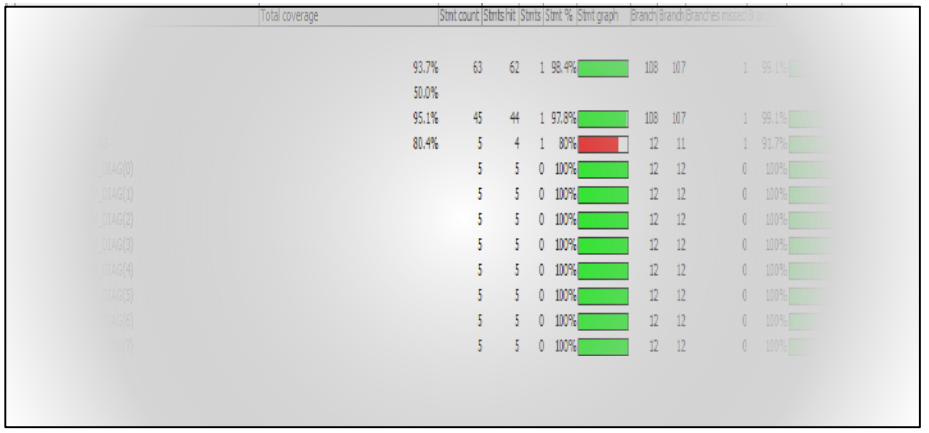


- The Result of Functional Test

SIGNAL	status	value	expt	p/np	SWR
reset	input	1	n/a	n/a	15
SEL_SBUS	input	1	n/a	n/a	15
SLOT_POS	input	0	n/a	n/a	15
SBXD	input	1111	n/a	n/a	15
id_module	input	46c1	n/a	n/a	15
sel_bus	output	0	0	Pass	15
err_sel_bus	output	0	0	Pass	15
err_proc	output	0	0	Pass	15
err_srk	output	0	0	Pass	15
err_tx_scan	output	0	0	Pass	15
norm_op	output	0	0	Pass	15
clr_errst	output	0	0	Pass	15
en_cmd_set	output	0	0	Pass	15
set_scan_time	output	ffffa	ffffa	Pass	15
set_en_tx_diag	output	0	0	Pass	15
set_en_tx_ch	output	0	0	Pass	15
set_en_rx_diag	output	0	0	Pass	15
set_en_rx_ch	output	0	0	Pass	15
set_tx_sadr0-3	output	ffff	ffff	Pass	15
set_tx_madr0-3	output	ffff	ffff	Pass	15
set_tx_dlen0-3	output	80	80	Pass	15
set_tx_scant0-3	output	ffffa	ffffa	Pass	15
set_rx_sadr0-3	output	ffff	ffff	Pass	15
set_rx_madr0-3	output	ffff	ffff	Pass	15
set_rx_dlen0-3	output	80	80	Pass	15
sta_op_count	output	0	0	Pass	15
drdy_tx_dgm	output	0	0	Pass	15

(value : actual I/O, expt: expected value, p/np : True/False

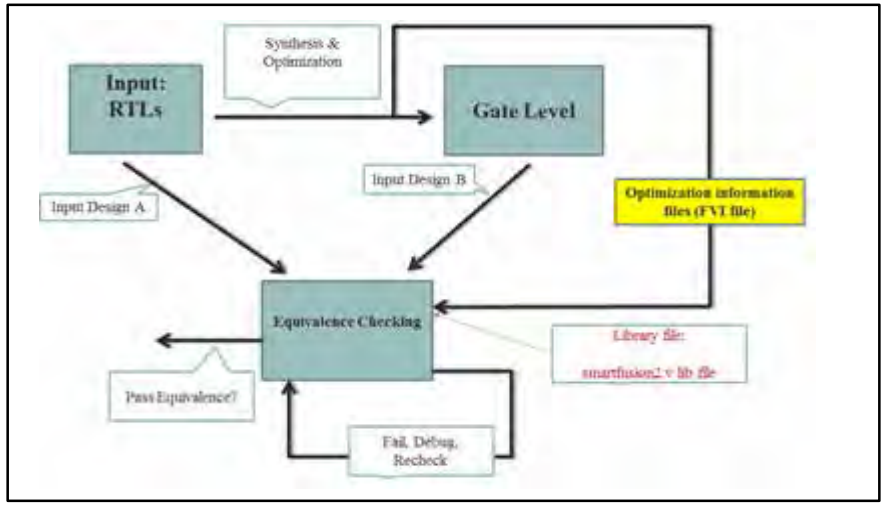
- The Result of Code Coverage Analysis



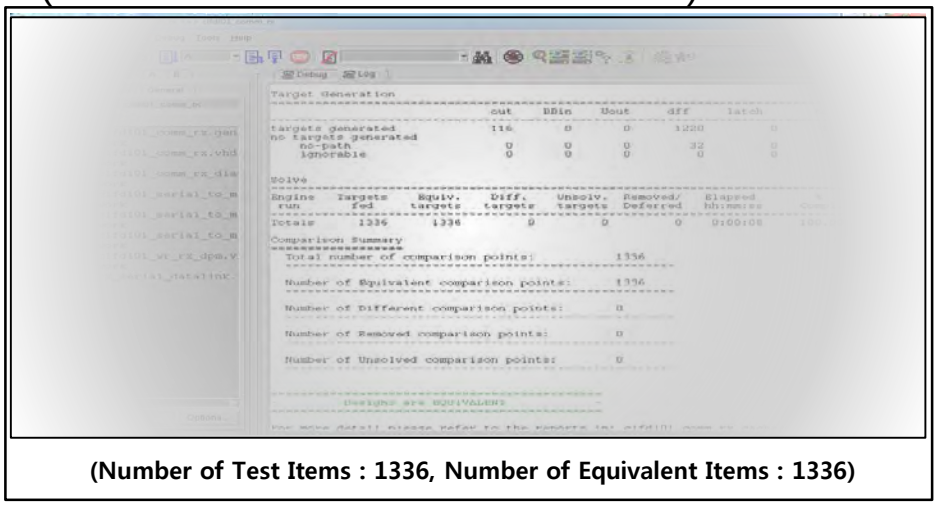
2. V&V and Testing:detail output example

2-2. Component Test

- Method of Equivalent Checking

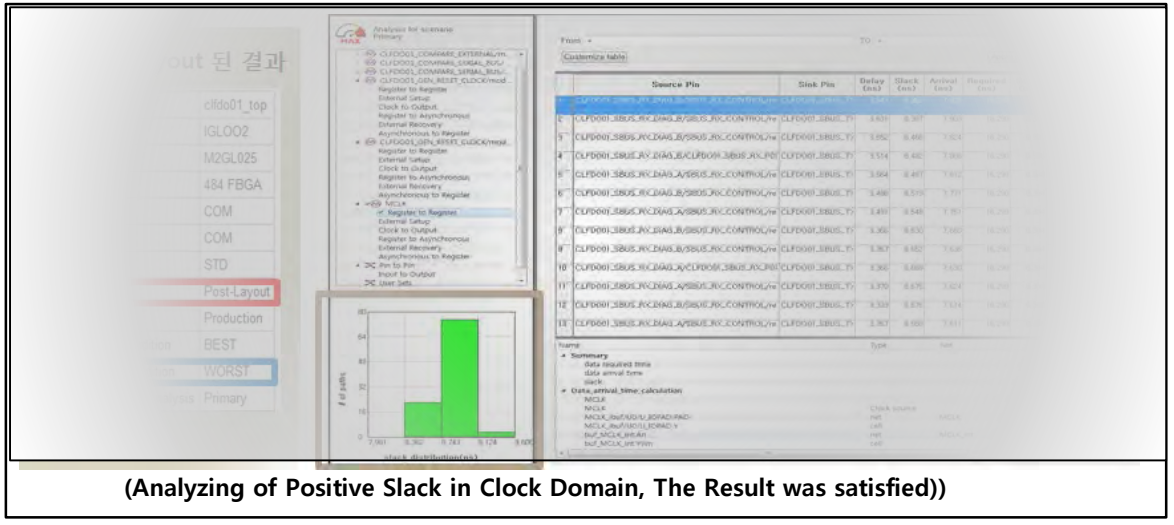


- The Result of Equivalent Checking
  (Ex : Data Link Communication Module)



(Number of Test Items : 1336, Number of Equivalent Items : 1336)

- **Result of Static Timing Analysis (Using SmartTime Tool)**

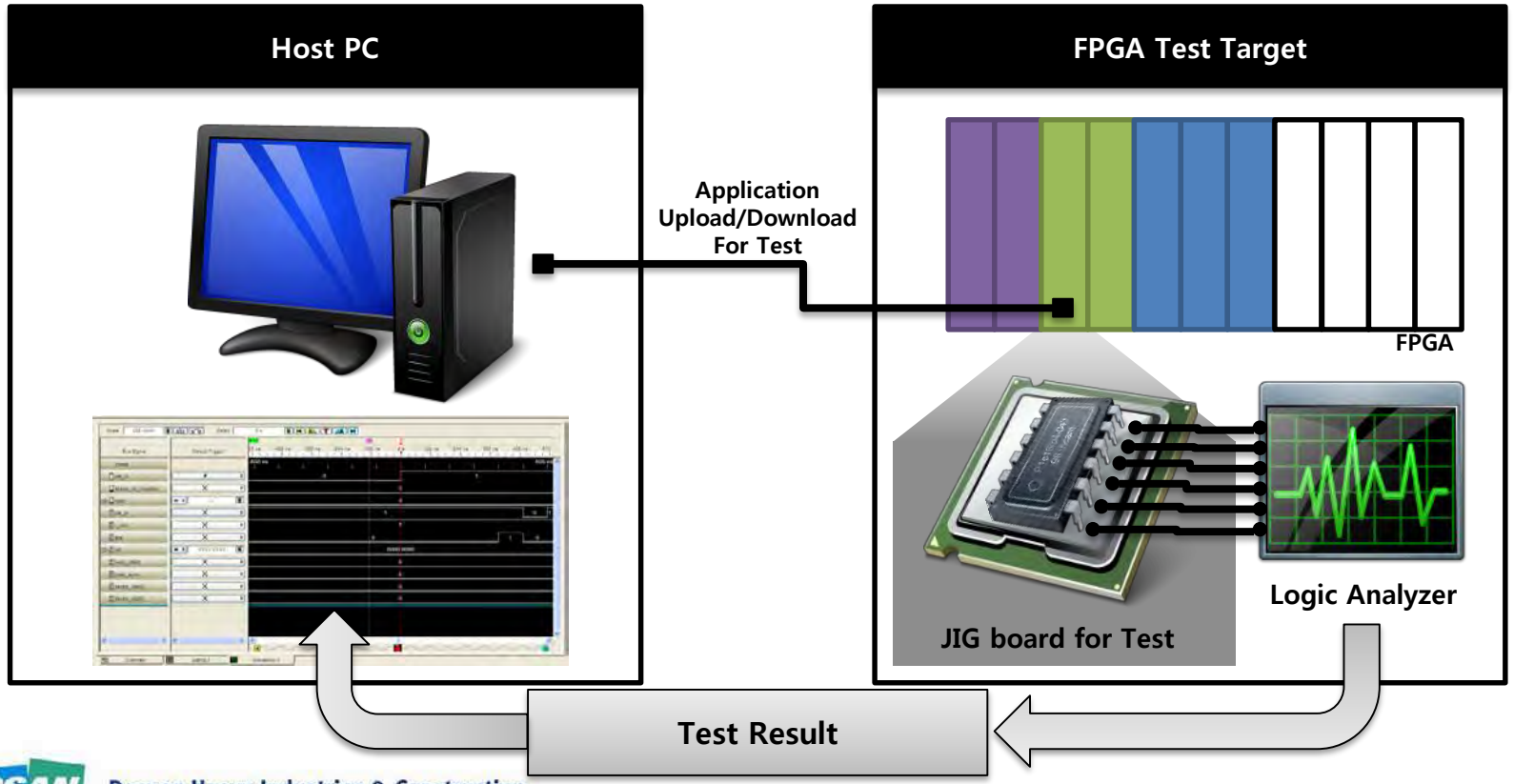


(Analyzing of Positive Slack in Clock Domain, The Result was satisfied))

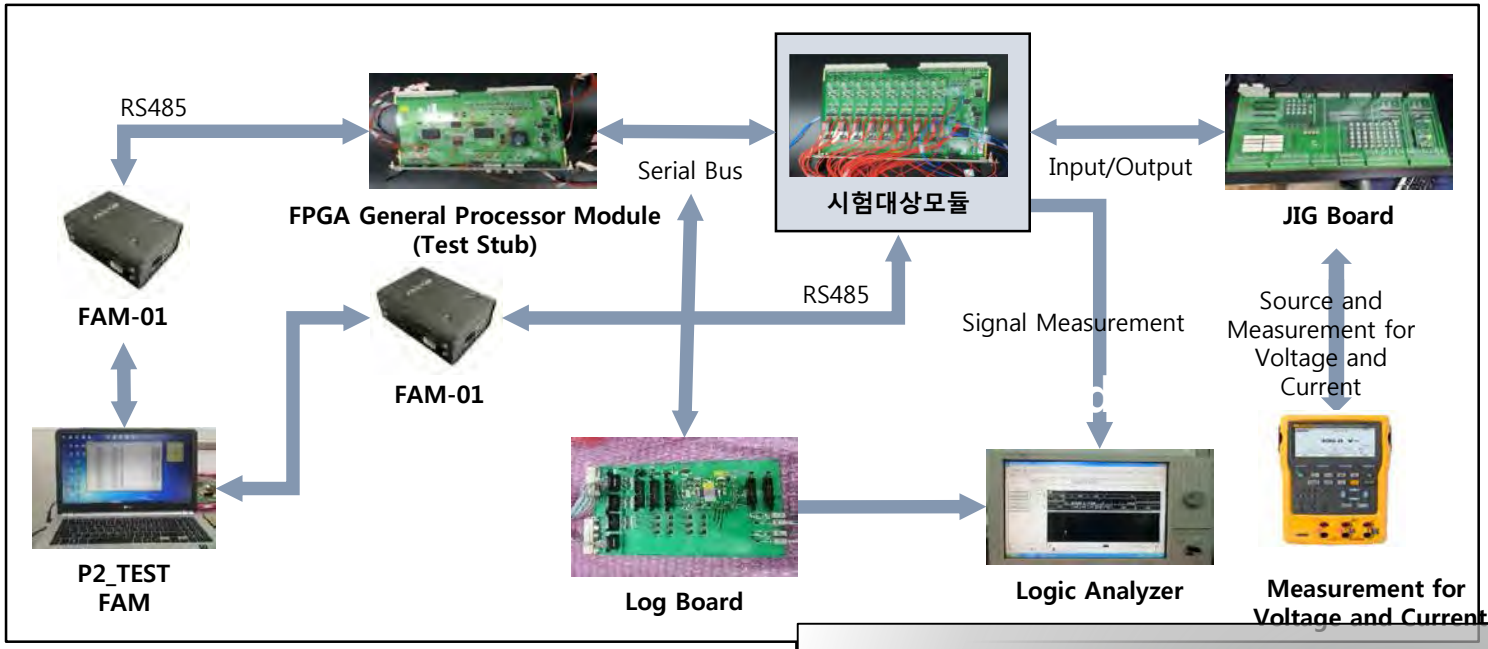
2. V&V and Testing
2-3. Integration Test

Requirement Verification | Design Verification | Code Inspection / Component Test | **Integration (card, module) Test** | System (FPGA controller) Test

- FPGA verification using hardware signal triggering and monitoring
- Test criteria : Requirement coverage
- Test environment : Jig board and signal jumpers for monitoring



2. V&V and Testing
2-3. Integration Test



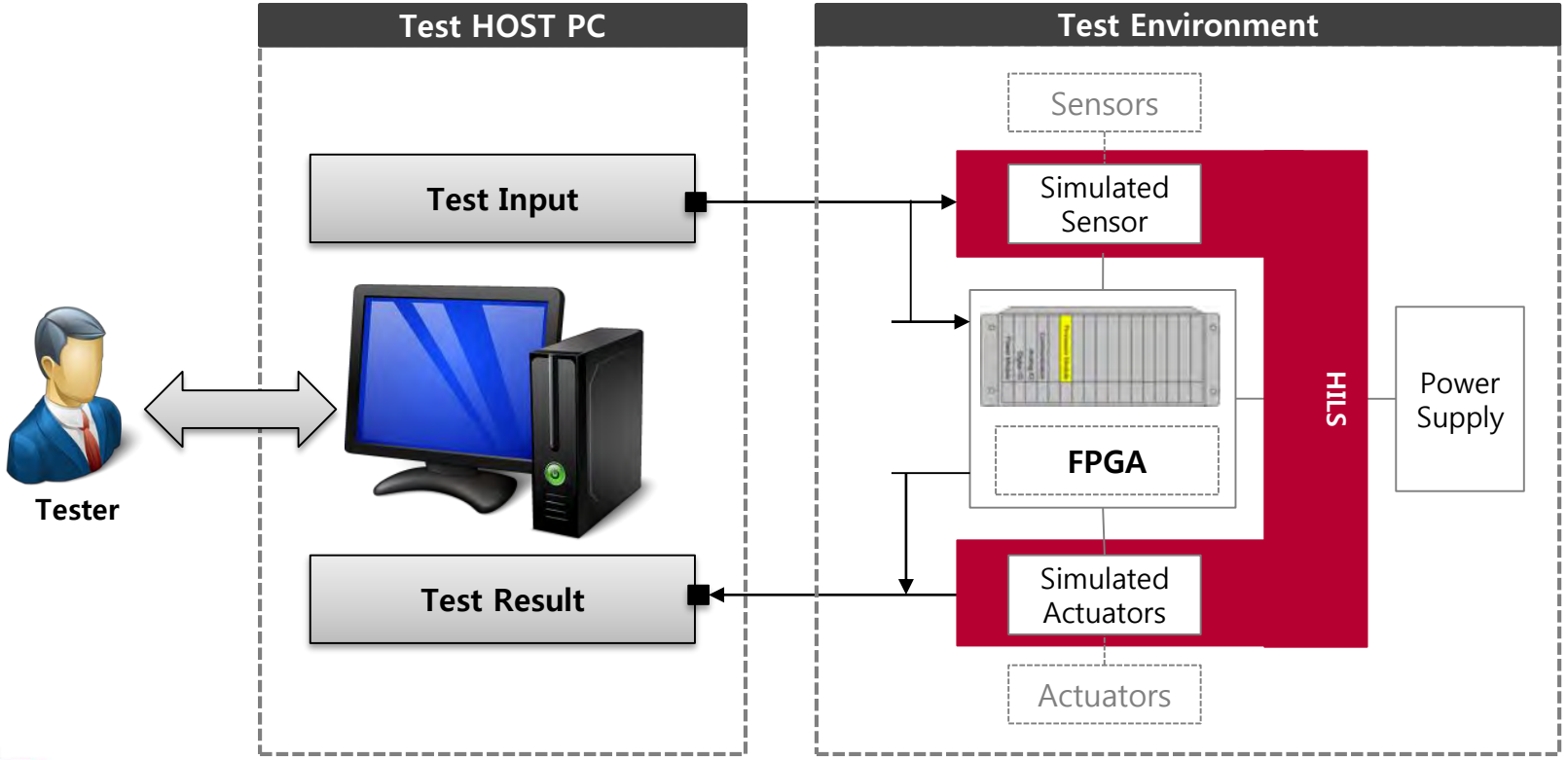
◄ Test Environment for I/O Module Integration Test

The Execution for I/O Module Integration Test ►

2. V&V and Testing
2-4. System Test

Requirement Verification | Design Verification | Code Inspection / Component Test | Integration (card, module) Test | **System (FPGA controller) Test**

- **Validated by Hardware-in-the-loop simulation**
- **Test criteria : Requirement coverage**
- **Test environment : Hardware-in-the-loop simulation environment**



2. V&V and Testing

2-4. System Test

Requirement Verification | Design Verification | Code Inspection / Component Test | Integration (card, module) Test | System (FPGA controller) Test

Tester

SRS

Analysis Result

Analysis

Input / Output Identification

Test case Design

Test Case

Test Execution

Result Analysis

Result Reporting

Test Case Addition

- System Test
  - Functional Test
  - Performance Test
  - Interface Test
  - Real-time Test
  - Fault Injection Test
  - Scenario based Test

Requirement Verification | Design Verification | Code Inspection / Component Test | Integration (card, module) Test | **System (FPGA controller) Test**

1. **Platform Qualification**

   - Y=aX Linear Function : Full Range Test (10,000)

2. **Manual Test before Automatic Testing**

   - Fluke 754, Graphic Record

3. **I/O Combination Test (AI-AO, DI-DO, DI-FDL-GP-F D L-DO)**

4. **Scenario based automatic testing after Satisfying of 1,2 and 3 conditions**

   1) Functional (Triangle Wave : 0-Increment-peack-decrement-0): 10,000 Test Case

   2) Performance (Input:25ms –GP –output:50ms : Closed Loop BACK PASS/FAIL)

   3) Real-time (2ms~1000ms :25ms, 50ms, 500ms etc.)

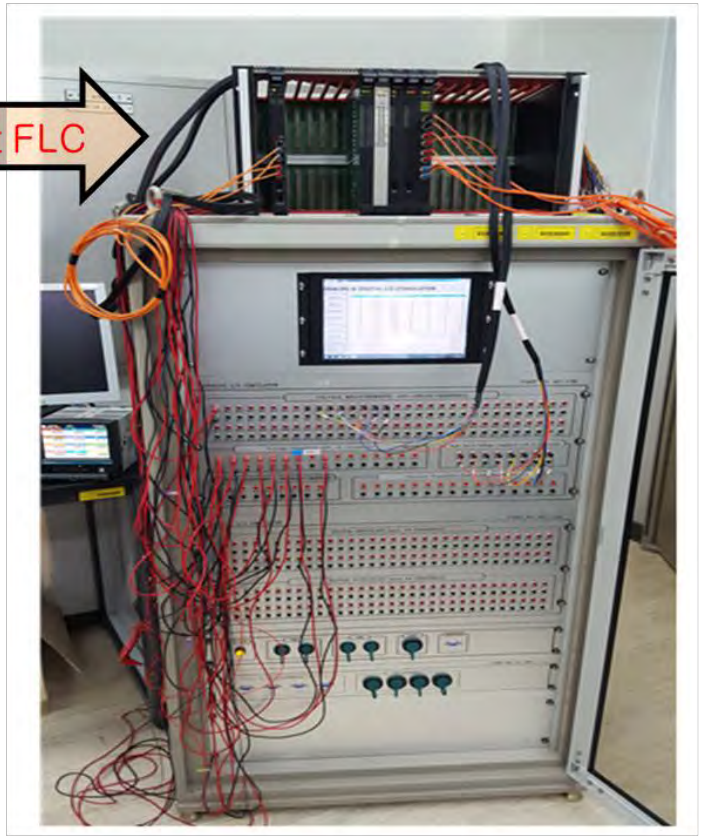
   4) Accuracy : 0.01% tolerance

5. **Analysis of Test Result**

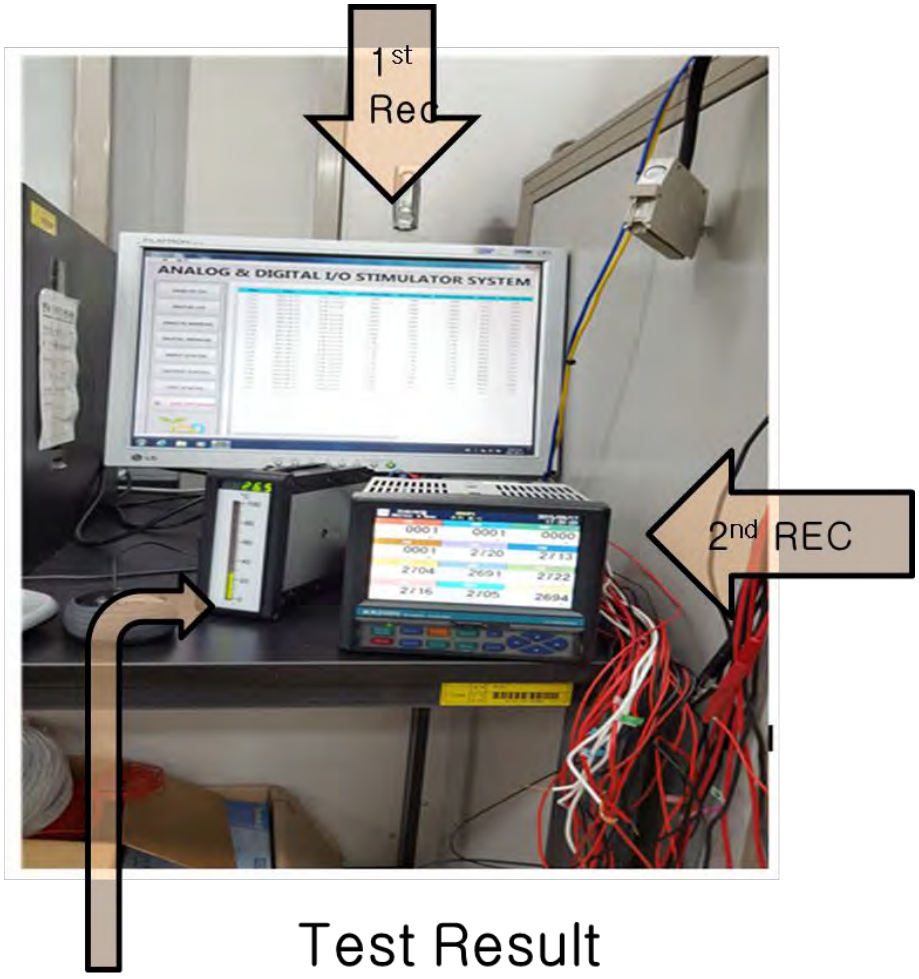
2. V&V and Testing

2-4. System Test

Requirement Verification | Design Verification | Code Inspection / Component Test | Integration (card, module) Test | **System (FPGA controller) Test**



Automatic Signal Generator



Test Result

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3. Recommendation

- ***Let's share practice & ideas for peaceful use of Nuclear Energy***

  ----- Objective/Mission of IAEA, President D. Eisenhower

- ***To lead Nuclear Renaissance again***

Thank you for listening

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