



Introduction to the I&C group at EDF SEPTEN and its activities

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The I&C team of EDF SEPTEN - Missions



Responsible for the software qualification of...



Class 1 systems

Class 2 & 3 platforms

Smartdevices

IAEA NS-G-1.3		Systems Important to Safety			Systems not important to safety	
		Safety	Safety-related			
IAEA SSG-30	Function	Safety category 1	Safety category 2	Safety category 3		
	System	Safety class 1	Safety class 2	Safety class 3		
Systems Important to Safety						
IEC 61226	I&C function	Category A	Category B	Category C	Non-classified	
	I&C system	Class 1	Class 2	Class 3		
IEEE		Systems Important to Safety			Non-safety-related	
		Safety-related	s			
EUR ⁶	Safety level of functions / I&C systems	F1A	F1B	F2	NS (non-safety)	
<i>MDEP member states</i>						
Canada		Category 1	Category 2	Category 3	Category 4	
France		F1A	F1B	F2	Non-classified	
Finland		Class 2	Class 3	EYT/ STUK	EYT (classified non-nuclear)	
UK		Class 1	Class 2	Class 3	Non-classified	
United States		Systems Important to Safety			(not specified)	
		Safety-Related	s			
India		IA	IB	IC	NINS	
Japan		PS1/MS1		PS2/MS2	PS3/MS3	Non-nuclear safety
Korea		IC-1		IC-2	IC-3	
Russia		Class 2	Class 3		Class 4 (Systems not important to safety)	
<i>Others nuclear states</i>						
Switzerland		1	2	3	Non-classified	
Germany	I&C function	Category 1	Category 2	Category 3	Non-classified	
	I&C equipment	E1		E2		



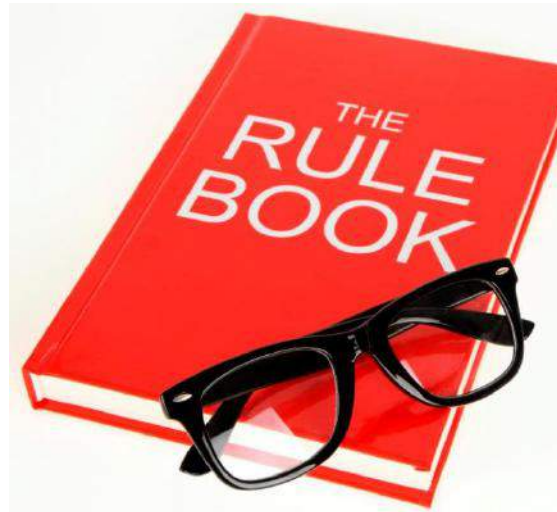
IAEA NS-G-1.3		Systems Important to Safety			
	Function	Safety category 1	Category 3		Systems not important to safety
	System	Safety class 1	Class 3		
	I&C function	Category A	Category C		Non-classified
	I&C system	Class 1	Class 3		
		Safety-related			Non-safety-related
EUR ⁶	Level of I&C	F1A			NS (non-safety)
<i>MDEP member states</i>					
Canada		Category 1	Category 3		Category 4
France		F1A	F1B	F2	Non-classified
Finland		Class 2	Class 3	EYT/ STUK	EYT (classified non-nuclear)
UK		Class 1	Class 2	Class 3	Non-classified
Systems Important to Safety					
	ated				(not specified)
		IB	IC		NINS
	/MS1	PS2/MS2	PS3/MS3		Non-nuclear safety
	>-1	IC-2			IC-3
		Class 3			Class 4 (Systems not important to safety)
		2	3		Non-classified
Germany	I&C function	Category 1	Category 2	Category 3	Non-classified
	I&C equipment	E1		E2	



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Software and hardware qualification EDF technical rules

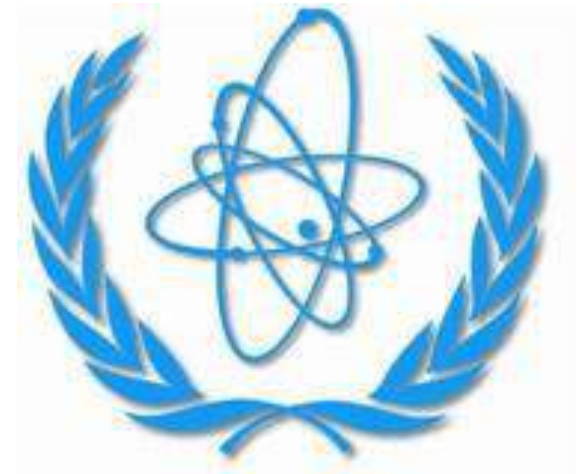


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National and international codes and standards

afcen



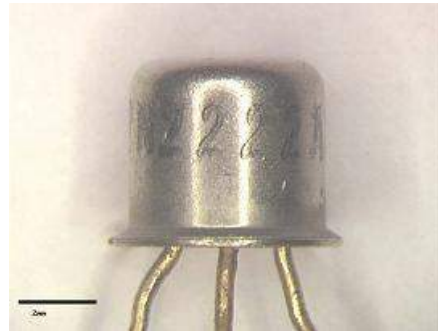
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R&D strategy and activity management

```

public class Program {
    public Integer next() {
        for(int i = p.length - 1; i >= 0;
            i--) {
            if (++p[i] > n)
                p[i] = nextInteger(0);
            else
                return p;
        }
        throw new NoSuchElementException();
    }
}
    
```



```

library IEEE;
use IEEE.Std_Logic_1640.ALL;
use IEEE.Std_Logic_1875.ALL;
use IEEE.Std_Logic_Unsigned.ALL;

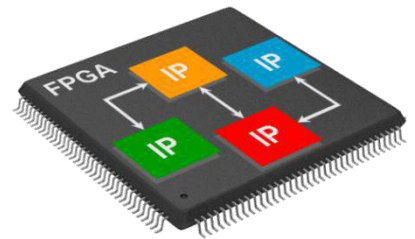
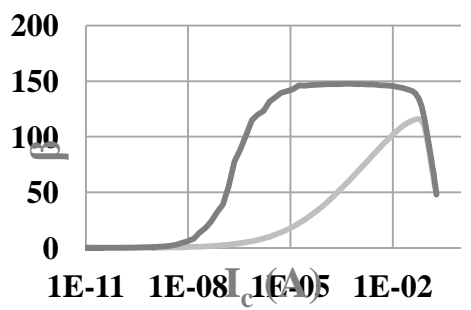
entity Test_Counter_VHDL is
    Port (
        Clk_xxxHz : in Std_Logic;
        Step_Clk : in Std_Logic;
        Select_Clk : in Std_Logic;
        Clk_Count_Enable : in Std_Logic;
        Bcd0_Bcd1_Bcd2_Bcd3 : out Std_Logic_Vector(3 downto 0));
end Test_Counter_VHDL;

architecture Behavioral of Test_Counter_VHDL is
    Signal Q : Std_Logic_Vector(15 downto 0);
    Signal Clk : Std_Logic;

begin
    -- 2-bit multiplexer: Clk_xxx or Step_Clk = (Bstn0)
    Clk <= Clk_xxxHz when Select_Clk='1' else
        Step_Clk;

    process (Clk, Clr)
    begin
        if Clr='1' then
            Q <= (others => '0'); -- "0000000000000000"
        elsif rising_edge(Clk) then
            if Count_Enable='1' then
                Q <= Q + 1;
            end if;
        end process;

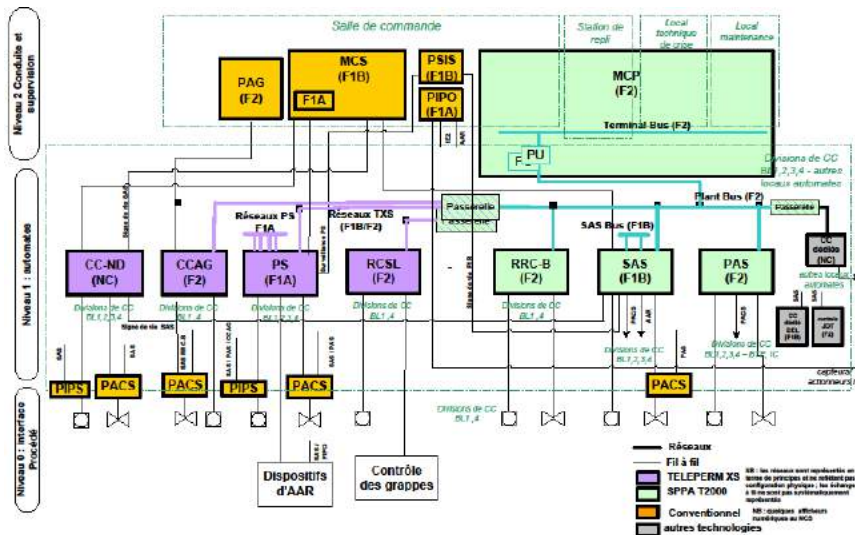
        Bcd3 <= Q(15 downto 12);
        Bcd2 <= Q(11 downto 8);
        Bcd1 <= Q(7 downto 4);
        Bcd0 <= Q(3 downto 0);
    end Behavioral;
end;
    
```



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Expertise on I&C architectures and technologies



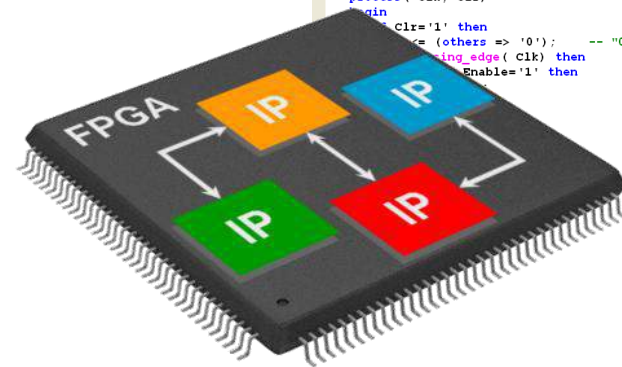
```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Test_Counter_VHDL is
    Port (
        Clk_xxxHz : in std_logic;
        Step_Clk : in std_logic;
        Select_Clk : in std_logic;
        Clr, Count_Enable : in std_logic;
        Bcd0, Bcd1, Bcd2, Bcd3 : out std_logic_vector(3 downto 0));
end Test_Counter_VHDL;

architecture Behavioral of Test_Counter_VHDL is
    Signal Q : std_logic_vector( 15 downto 0);
    Signal Clk : std_logic;
begin
    -- 2x8bit multiplexer: Clk_xxx or Step_Clk = [Btm0]
    Clk <= Clk_xxxHz when Select_Clk='1' else
        Step_Clk;

    process (Clk, Clr)
    begin
        if Clr='1' then
            Q <= (others => '0'); -- "0000000000000000"
        elsif rising_edge (Clk) then
            Count_Enable='1' then
                Q <= Q + 1;
            end if;
        end if;
    end process;
end architecture Behavioral;
    
```



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I&C qualification and expertise for present and future fleet

