AGENDA

9th International Workshop on Application of Field Programmable Gate Arrays in Nuclear Power Plants

October 3-6, 2016, Lyon, France

hosted by EDF SEPTEN in cooperation with the IAEA and SunPort SA.

Day 1 – Monday, 3 October 2016		
Time	**Event**	**Speaker**
8:30 – 09:30	Registration	
Opening Session		
09:30 – 09:40	Welcome, Introduction & Agenda	Oszvald Glöckler SunPort SA
09:40 – 09:50	Message from EDF SEPTEN management	Guillaume Jacquart EDF SEPTEN
09:50– 10:00	Organizer's Welcome	Alexander Wigg EDF SEPTEN
10:00– 10:15	IAEA Welcome	János Eiler IAEA
10:15 – 10:30	Introduction to the I&C group at EDF SEPTEN and its activities	Ludovic Pietre-Cambacedes I&C Group Manager, EDF SEPTEN
10:30 – 11:00	Coffee Break	
11:00 – 11:30	Invited Presentation: New IAEA publication on the application of FPGAs in NPP I&C systems	János Eiler IAEA
11:30 – 12:00	Invited Presentation: A case for the adoption of FPGA technology in the implementation and replacement of equipment and systems in NPPs	Sergio Russomanno SunPort SA
12:00 – 12:30	Group Photo	
12:30 – 14:00	Lunch Break	
Technical Session on Systems & Applications		**Chair: Alexander Wigg**
14:00 – 14:30	FPGAs in safety related applications in Nordic countries	Sofia Guerra, Samual George Adelard LLP
14:30 – 15:00	FPGA & µProcessor based platforms: Taking and sharing benefits from both worlds	Julien Bach Rolls-Royce

15:00 – 15:30	Development of DI&C Technology to improve Analog Equipment with Digital System in Operating NPPs	Chae Ho Nam DOOSAN
15:30 – 16:00	Coffee Break	
16:00	City Tour	

Day 2 – Tuesday, 4 October 2016		
Time	**Event**	**Speaker**
Technical Session on Design		**Chair: Sergio Russomanno**
09:30 – 10:00	Evolution of safety design approaches: Radiy's experience	Kostiantyn Leontiiev RPC Radiy
10:00 – 10:30	FPGA-based I&C systems – unraveling myths from reality	Alexander Wigg EDF SEPTEN
10:30 – 11:00	Coffee Break	
11:00 – 12:30	**Panel Discussion on** Technology or Design: Which is more important in the design of safety-classified I&C systems?	**Moderator:** **Alexander Wigg**
12:30 – 14:00	Lunch Break	
Technical Session on Studies, Modelling, and Testing		**Chair: Anton Andrashov**
14:00 – 14:30	Failure Mode Taxonomy for Assessing the Reliability of Field Programmable Gate Array Based Instrumentation and Control Systems	Phillip McNelles Canadian Nuclear Safety Commission, CNSC
14:30 – 15:00	Verification of FPGA application design by model checking	Antti Pakonen VTT Technical Research Centre of Finland Ltd
15:00 – 15:30	Coffee Break	
Technical Session on Certification, Qualification, and Standards		**Chair: Anton Andrashov**
15:30 – 16:00	Principles for FPGA based I&C platform redesign and class 2 qualification	Frederic Daumas EDF R&D
16:00 – 16:30	Development of a new IEC standard for HDL programmed integrated circuits for systems performing category B or C functions	Alexander Wigg EDF SEPTEN
16:30 – 17:00	Discussion	

Day 3 – Wednesday, 5 October 2016		
Time	**Event**	**Speaker**
Technical Session on Certification, Qualification, and Standards		**Chair: Oszvald Glöckler**
09:30 – 10:00	NRC Topical Report Certification Process: Suggestions for Success	Mark Burzynski NewClear Day, Inc
10:00 – 10:30	Certification of RadICS platform as per US NRC requirements	Anton Andrashov RadICS LLC
10:30 – 11:00	Coffee Break	
11:00 – 12:30	**Panel Discussion** on Regulations, Licensing, and Standards of FPGA Applications	**Moderator:** **Mark Burzynski**
12:30 – 14:00	Lunch Break	
Technical Session on Platforms		**Chair: János Eiler**
14:00 – 14:30	A Study on NicSys®8000N's HAF601 Licensing Process	Wanwan SHEN CNCS
14:30 – 15:00	Isolation and independence principles used in the design of the FPGA-based safety I&C platform NicSys8000N	Chenghua LIANG CNCS
15:00 – 15:30	Algorithm configuration functions of the FPGA-based safety I&C platform NicSys8000N designed for developing engineering applications	Qinfeng WANG CNCS
15:30 – 16:00	Coffee Break	
16:00 – 16:30	FPGA Version of HFC-6000 Platform	Steve Yang Doosan HF Controls
16:30 – 17:00	Introduction of Class 1 FPGA Platform for the UK ABWR	Hideo Harada Hitachi
17:00 – 17:30	Discussion	
19:30	Gala Dinner at Brasserie Léon de Lyon	

Day 4 – Thursday, 6 October 2016		
Time	**Event**	
09:30 – 10:00	CPLD development with Nuclear requirements - reliability feedback on 10 years	Perrenot Nicolas NEXEYA
10:00 – 11:30	**Panel Discussion on Development tools and processes for FPGA applications**	**Moderator: Sergio Russomanno**
11:30 – 12:00	Discussion on FPGAs in general; recommendations, and future activities Closing	All
12:00	Lunch	