中核控制系统工程有限公司
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CNCS

A research on design method of using FPGA to implement safety-critical system in NPPS

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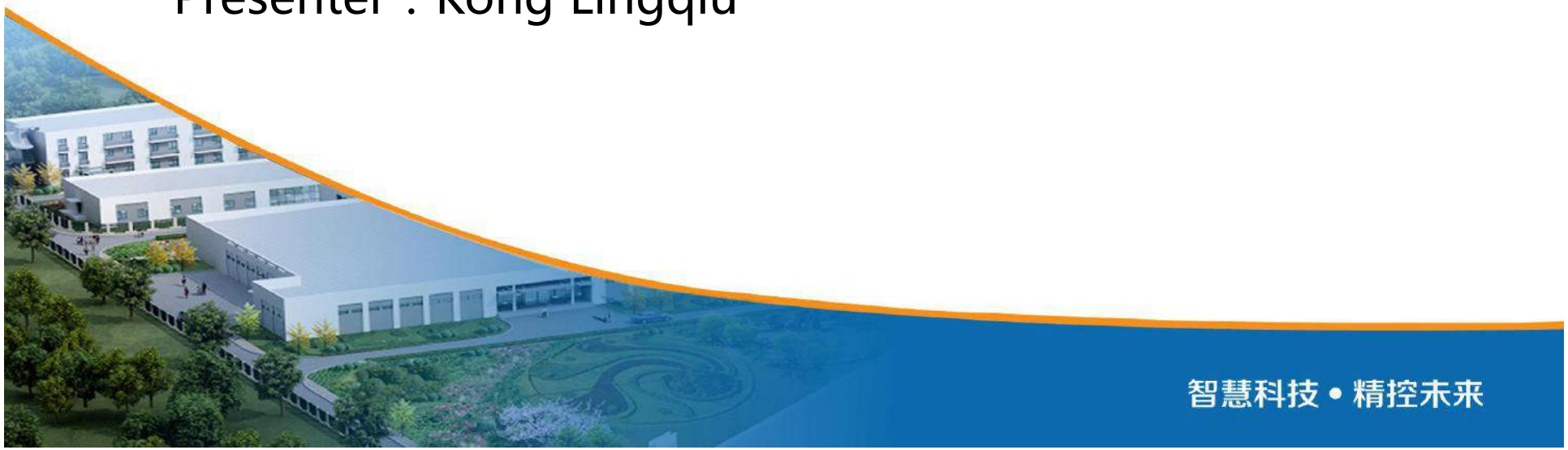

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OUTLINE

1. Background
2. Related technologies
3. Technical solutions
4. Conclusion
5. Q & A

1 Background (1/2)

- Nuclear safety systems commonly use CPU-based control mode currently.
- Using FPGA in the new generation of nuclear power safety systems is more and more widely.
- Brings new challenges:

Requirement for changing current engineer station staff's programming method, from their familiar DCS programming environment IEC61131- 3 language to Verilog language.

1 Background (2/2)

- CPU-based engineer station staff commonly adopt the language specified in the IEC61131-3 standard as their programming method.
- This article presents an FPGA-based implementation solution with programming interface following IEC61131-3 standard:
  - ✓ To achieve a smooth transition from CPU-based control mode to FPGA mode.
  - ✓ Don't have to change the engineer station staff's programming habits.
  - ✓ Maximize the reusing of the engineering staff's previous experience.

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2 Related technologies

- IEC61131-3 standard is the first international standard that provide standardized programming languages for the industrial control system
- Currently most industrial control languages follow this standard.

- Verilog HDL is a hardware description language.
- In texture format to describe the digital system's hardware structure and behavior, and can express the logic circuit diagram, logical expressions.
- It also can represent the logic functions implemented by the digital logic system.

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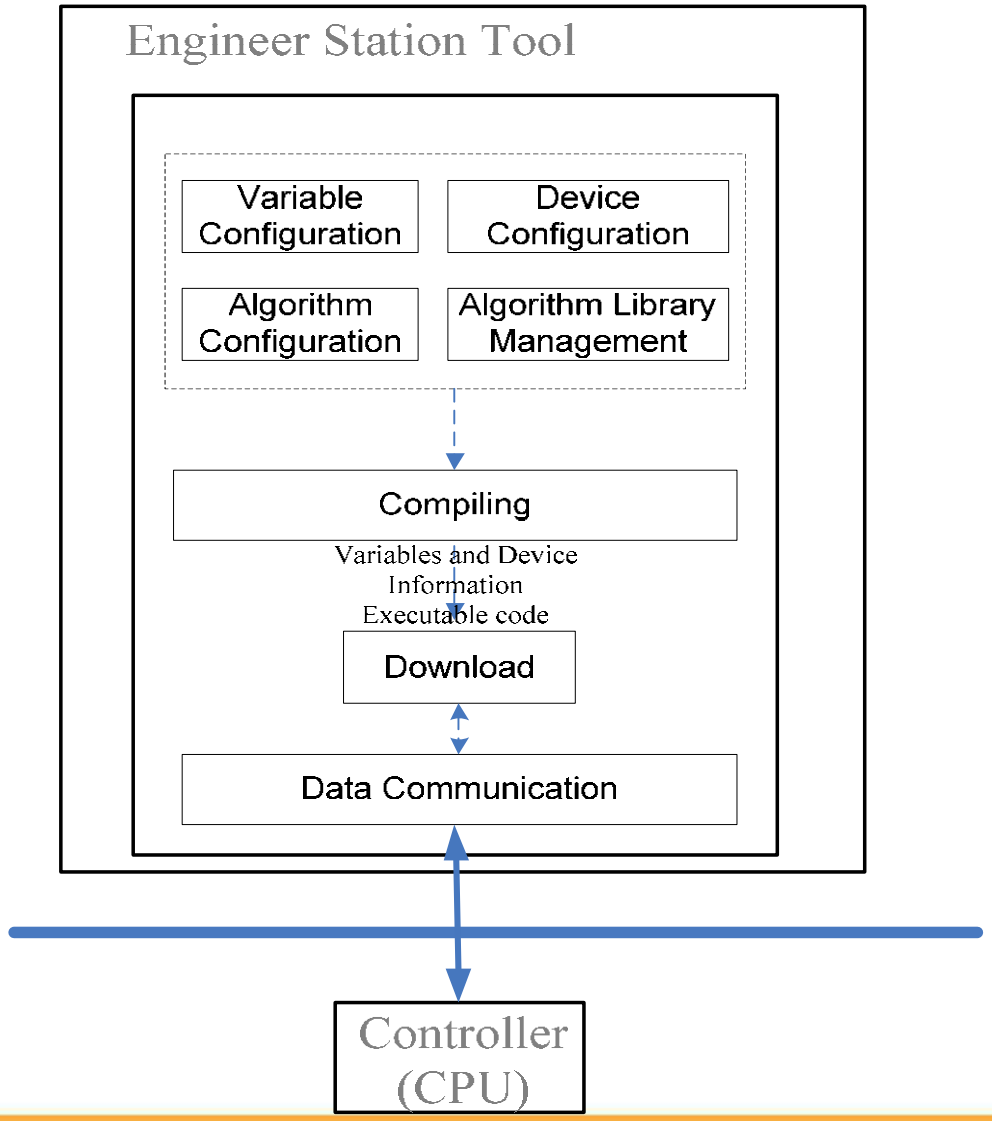
3 Technical solutions (1/11)

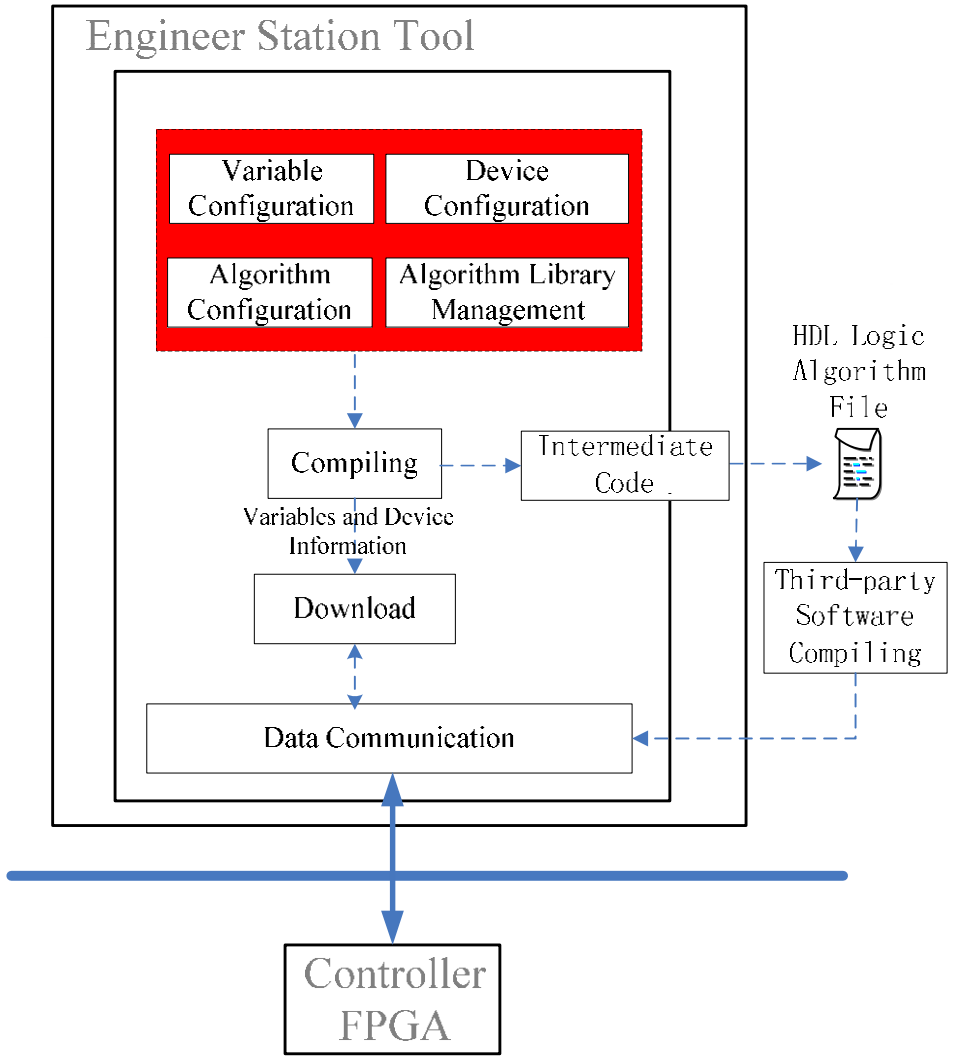
- Now engineer station tool software based on CPU controller are mostly developed by the language defined in IEC61131-3 standard in worldwide.



3 Technical solutions (2/11)

- The nuclear power plant safety control systems based on underlying FPGA technology require the engineering station staff to be familiar with Verilog language.
- Requires engineer station tools to provide the transaction process from IEC61131-3 standard language into Verilog language.
- In Verilog-based engineer station tool's development, it's very important to reuse current successful experience on CPU based system.

3 Technical solutions (3/11)



3 Technical solutions (4/11)

- The FPGA-based engineer station tool add the language converting part to CPU-based tool.
- Above implementation method doesn't have any influence on engineer station configuration staff:
  - ✓ No change in algorithm configuration, device configuration and variable configuration interface.
  - ✓ The compiling and checking method of configurations are the same as the CPU-based engineer station tool.
- Developers only need focus on the realization of language translation part to complete the development work.

3 Technical solutions (5/11)

- Comparing with the two architectures:
  - ✓ Retain the CPU-based architecture as basis of new architecture.
  - ✓ Add the underlying process of language translation in FPGA-based structure.
- For engineering station configuration staff:
  - ✓ Don’t have to re-learn Verilog HDL language.
  - ✓ The change of controller implementation method is transparent.
- For engineering station tool software’s developers:
  - ✓ CPU-based tools’ engineering practices, good stability and usability can be reused.
  - ✓ Can keep the functions of interface configuration part.

3 Technical solutions (6/11)

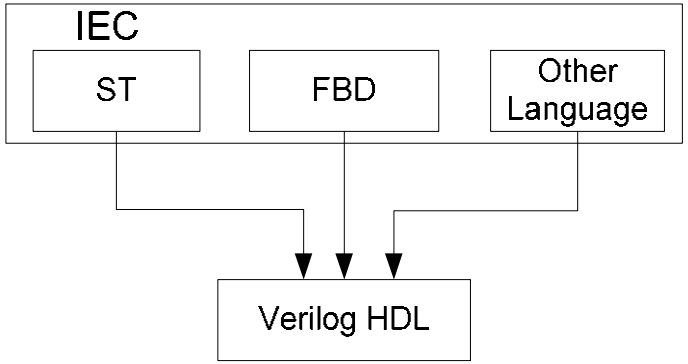
- Engineering configuration interface and pre-compile parts are same in two structures.
- Configuration interface part:
  - ✓ Algorithm configuration language supports ST and FBD
  - ✓ Variable configuration supports the basic data types and structure types defined in IEC 61131-3.
  - ✓ Device configuration shows the graphic configure interfaces.
- After completing configuration and pre-compiling, the tool compiles and downloads configuration information into the FPGA controller and run it.

3 Technical solutions (7/11)

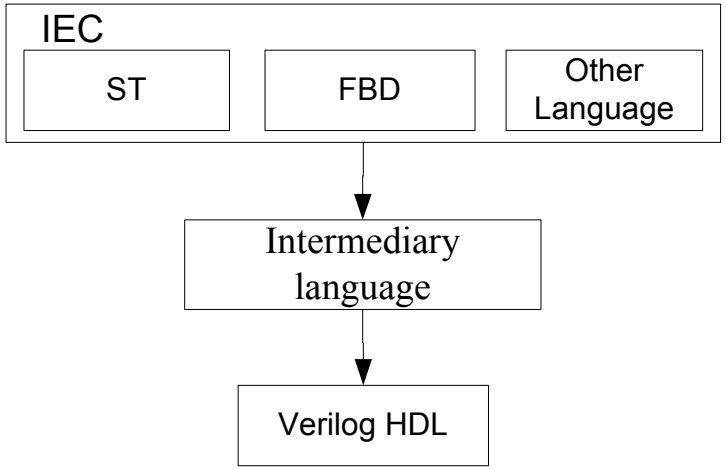
- The compiling and downloading processes of two structures are different:
- In CPU-based way, directly convert the algorithm configuration's content into the executable machine code and download.
- In FPGA-based way,
  - ✓ Translate the algorithm configuration into Verilog HDL.
  - ✓ Call the compiler specified by the FPGA device vendor to compile the Verilog HDL code.
  - ✓ Download the compiled information into the controllers to run.

3 Technical solutions (8/11)

- The conversion of algorithm configuration's textual language or graphic language into Verilog HDL language has the way right:



- Also has the conversion way right:

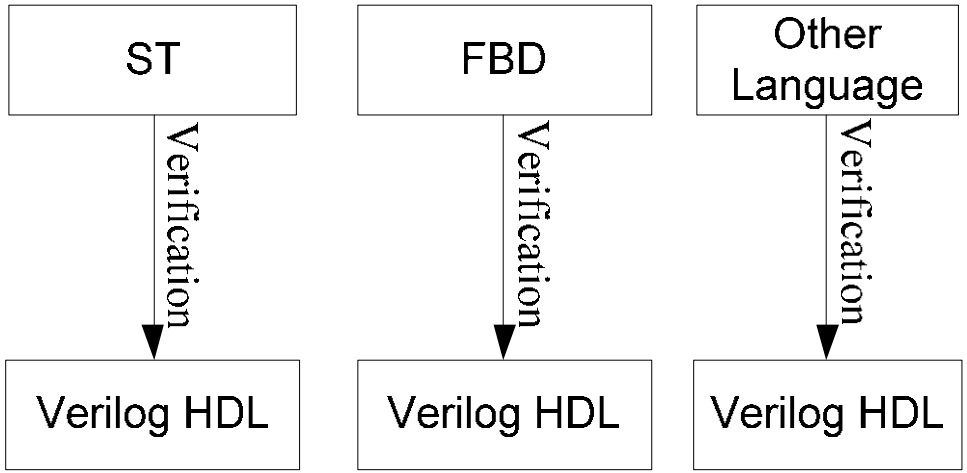


3 Technical solutions (9/11)

- We choose the second way with user-defined intermediary language:
  - ✓ Algorithm configuration uses the languages defined in IEC 61131-3 standard.
  - ✓ Convert the configurations into the intermediary language.
  - ✓ Then into Verilog HDL language.
- Main concerns of this design:
  - ✓ Reduce programming error probability.
  - ✓ Simplify the validation process of the software.

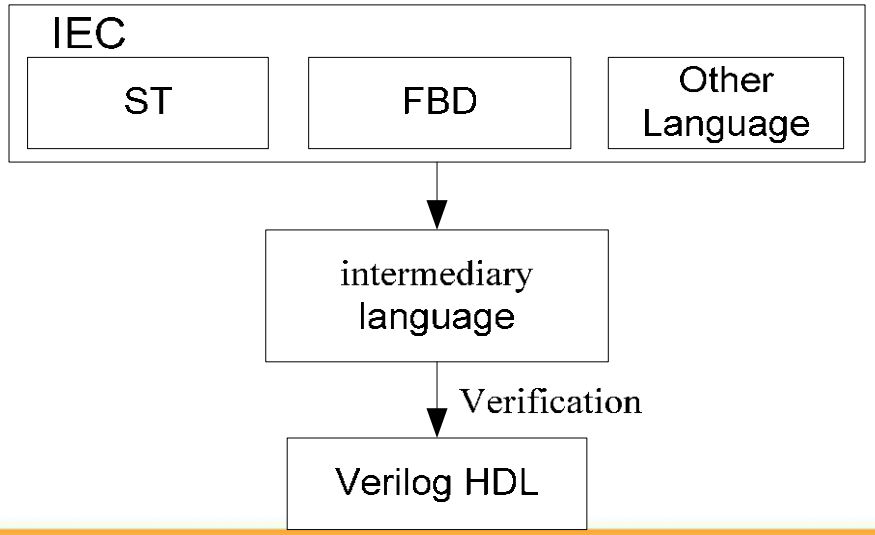
3 Technical solutions (10/11)

- In first method of conversion way:
  - ✓ Software developers should be familiar with Verilog HDL language.
  - ✓ Every configuration language's translation process must be verified.



3 Technical solutions (11/11)

- In second conversion way:
  - ✓ Uniformly convert IEC61131-3 language to a intermediary language.
  - ✓ Simplify the language verification.
  - ✓ Focus on verifying the correctness of translation from the intermediary language into Verilog HDL language



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4 Conclusion

- The FPGA-based architecture design has below advantages:
  - ✓ In the underlying code conversion way , translates IEC61131-3 language into HDL language.
  - ✓ It is transparent for engineer station staff no matter the underlying implementation way is the CPU controller or FPGA.
  - ✓ Engineer station tool software developers can reuse their most experiences in development of CPU-based engineer station tool.

THANKS FOR YOUR ATTENTION!

QUESTIONS?